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(30)Priority

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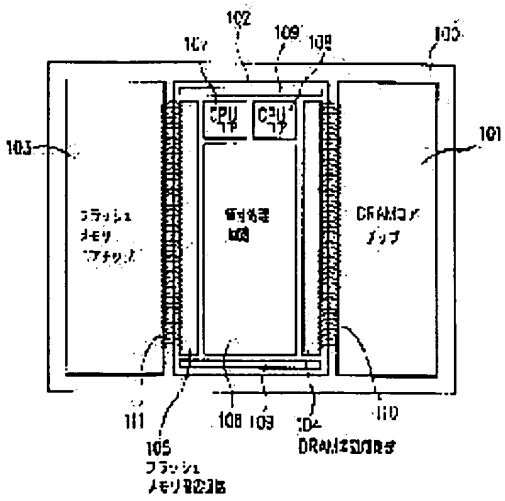
(54) SEMICONDUCTOR DEVICE, MANUFACTURE THEREOF, MEMORY CORE CHIP AND MEMORY PERIPHERAL CIRCUIT CHIP

(57)Abstract:

PURPOSE: To provide a low-cost semiconductor device which is operated at a low voltage with low power consumption.

CONSTITUTION: A semiconductor device comprises a plurality of circuit blocks having a first circuit block (DRAM core) and a second circuit block (DRAM peripheral circuit) having different block parameters such as design rules, wherein the first circuit block is formed on a first semiconductor chip (DRAM core chip)101, the second circuit block is formed on a second semiconductor chip 102, and electrically connected to the first circuit block. As a result, the semiconductor chips can be manufactured at low cost.



LEGAL STATUS

[Date of request for examination] 05.02.1998

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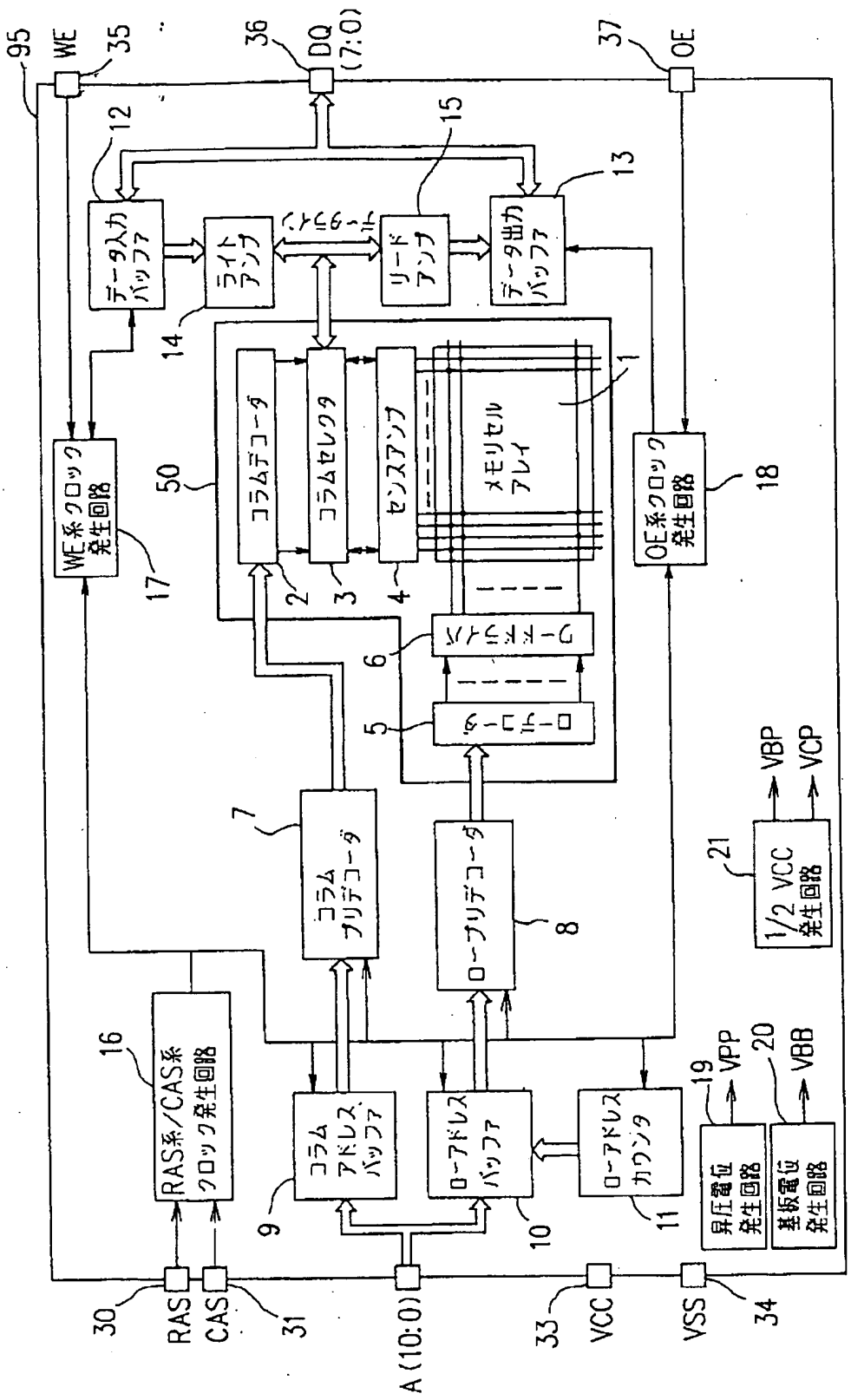
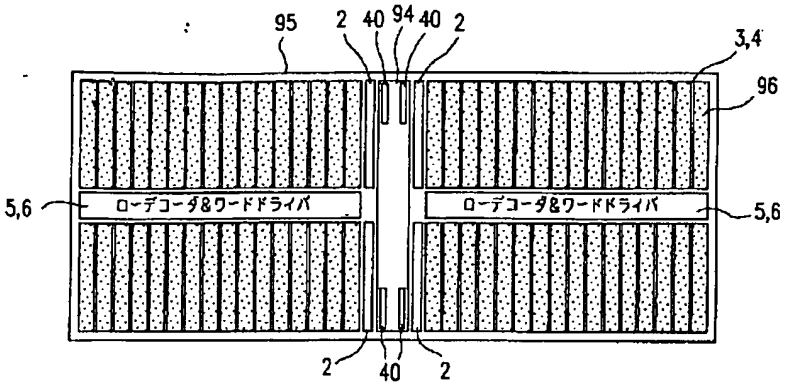
DRAWINGS

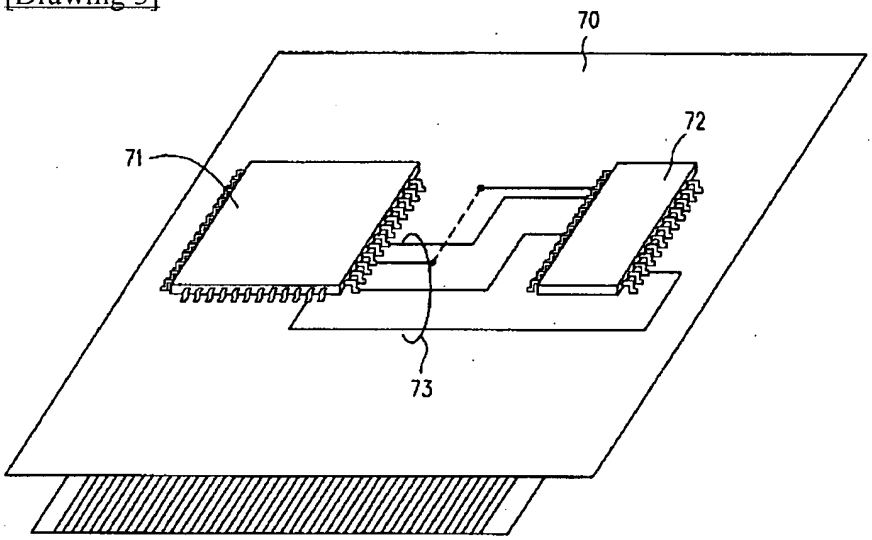
[Drawing 1]


95
WE
35
36
DQ (7:0)
37
OE
12
15
13
データ入力バッファ
ライトアンプ
リードアンプ
データ出力バッファ
14
1
WE系クロック発生回路
50
コラムデコーダ
コラムセレクタ
センスアンプ
メモリセルアレイ
OE系クロック発生回路
18
17
2
3
4
ワードドライバ
6
ロードライバ
5
7
コラムプリデコーダ
ローブリデコーダ
8
VBP
VCP
21
1/2 VCC発生回路
16
RAS系/CAS系クロック発生回路
コラムアドレスバッファ
ローアドレスバッファ
ローアドレスカウンタ
9
10
11
19
VPP
20
VBB
昇圧電位発生回路
基板電位発生回路
30
RAS
CAS
31
A (10:0)
33
VCC
VSS
34

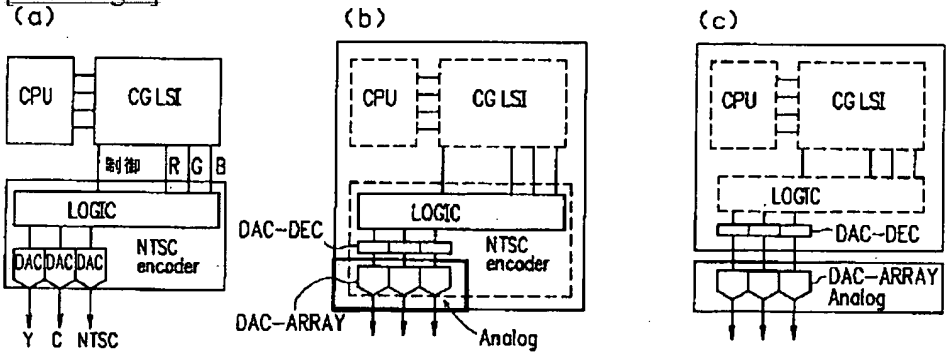
[Drawing 2]



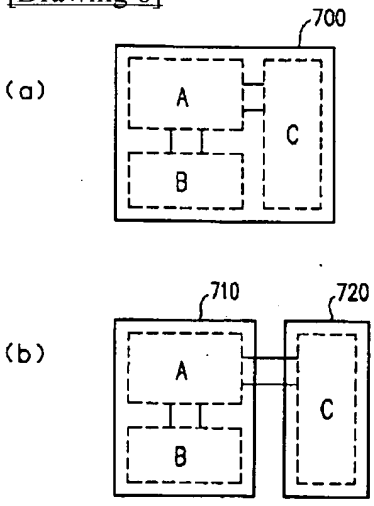
[Drawing 3]



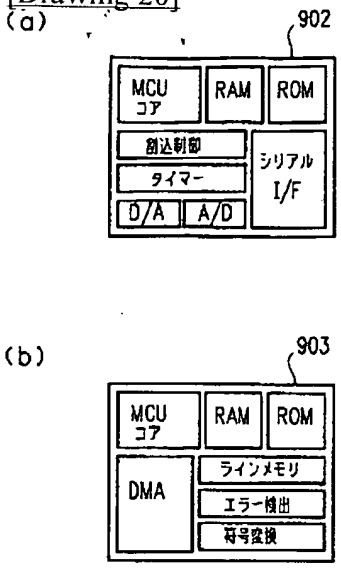
[Drawing 4]



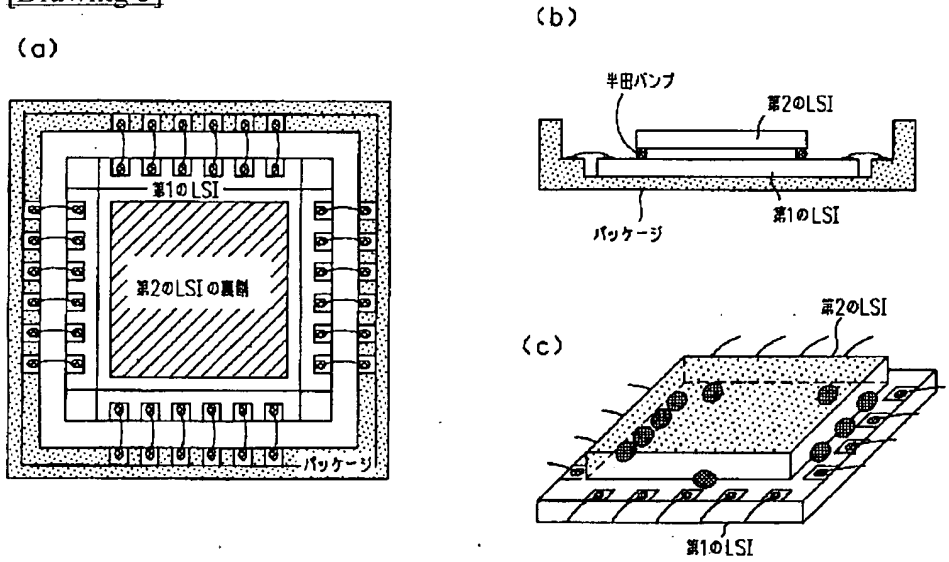
[Drawing 6]



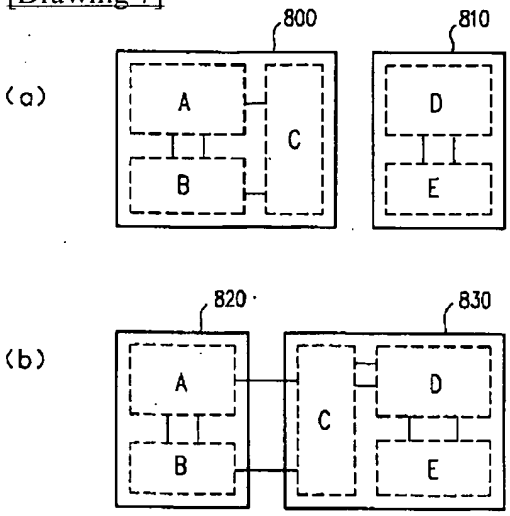
[Drawing 20]



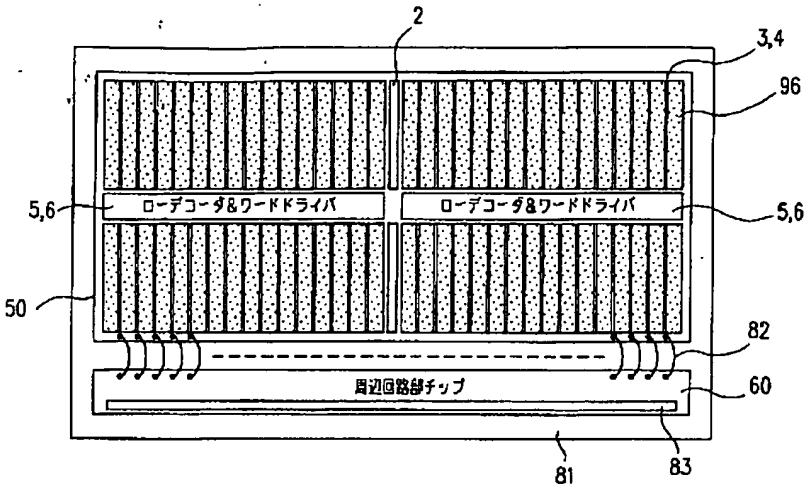
[Drawing 5]



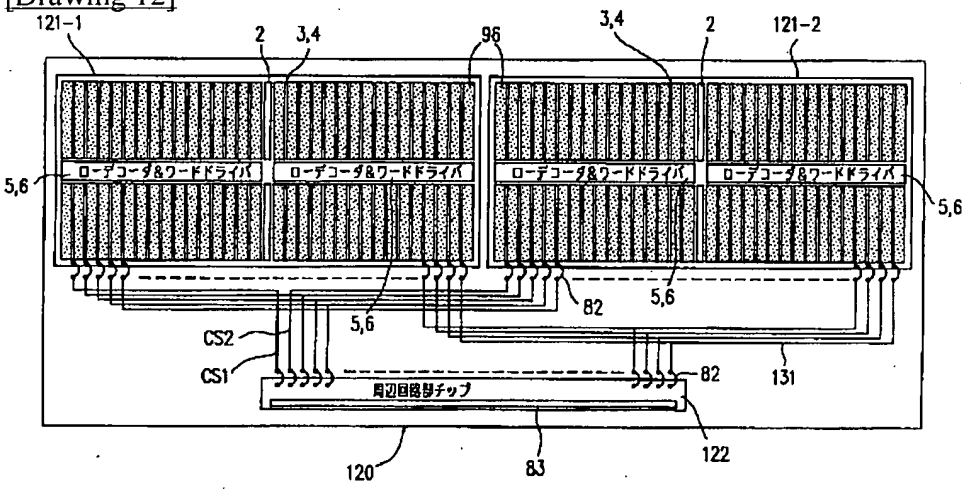
[Drawing 7]



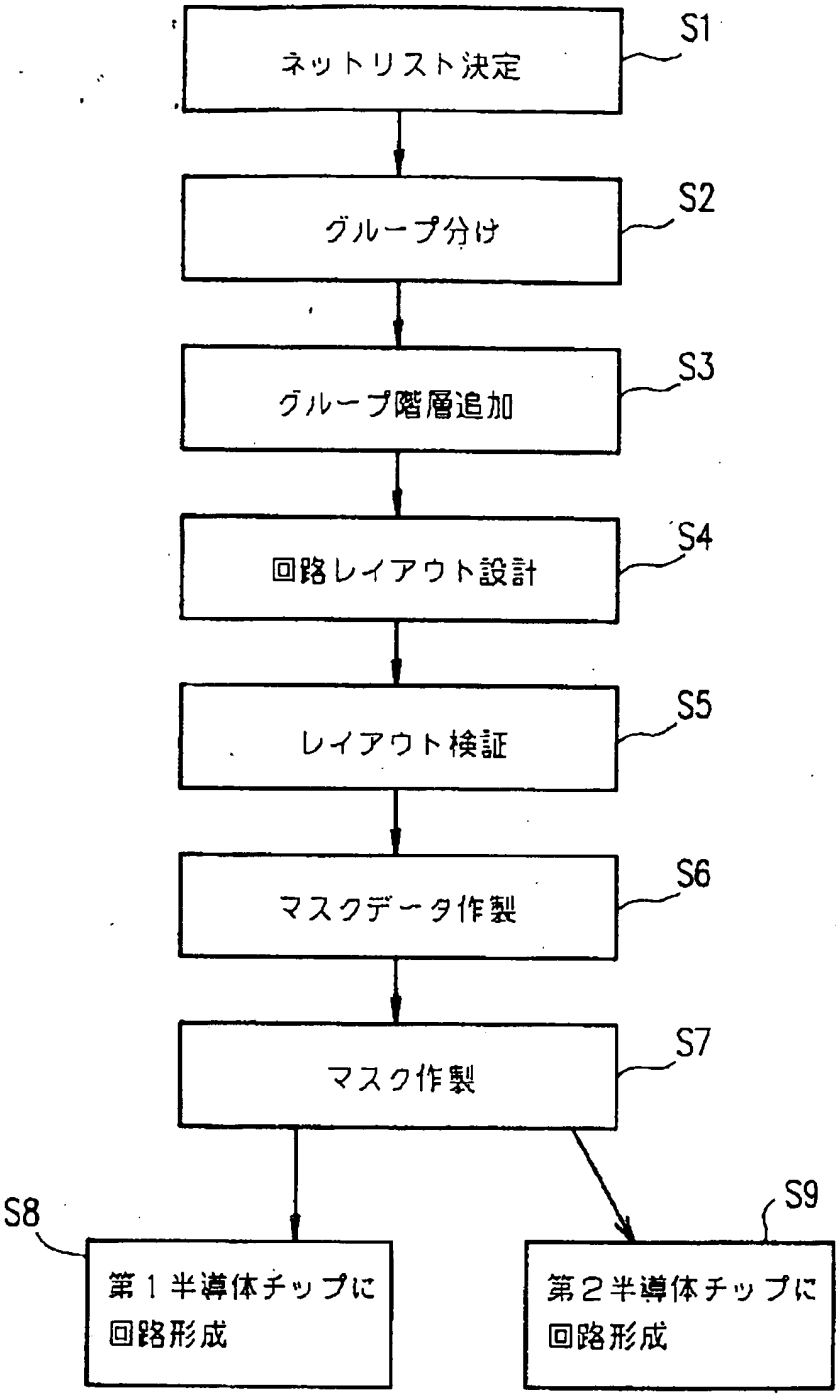
[Drawing 10]



[Drawing 12]

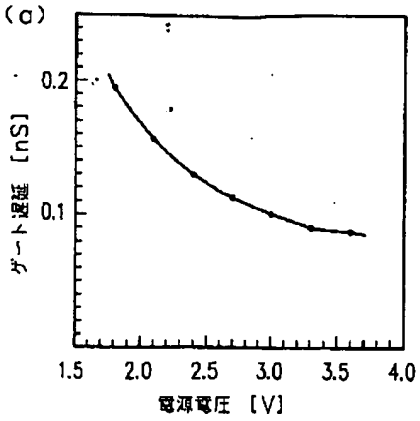


[Drawing 8]

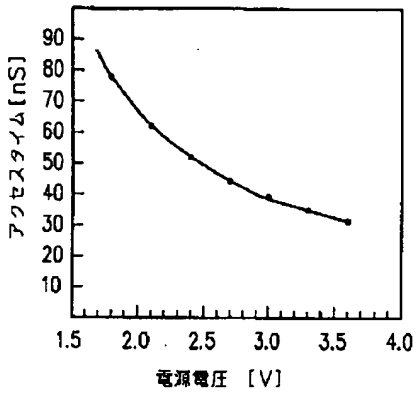

ネットリスト決定
S1
グループ分け
S2
グループ階層追加
S3
回路レイアウト設計
S4
レイアウト検証
S5
マスクデータ作製
S6
マスク作製
S7
S8
第１半導体チップに回路形成
S9
第２半導体チップに回路形成

[Drawing 16]

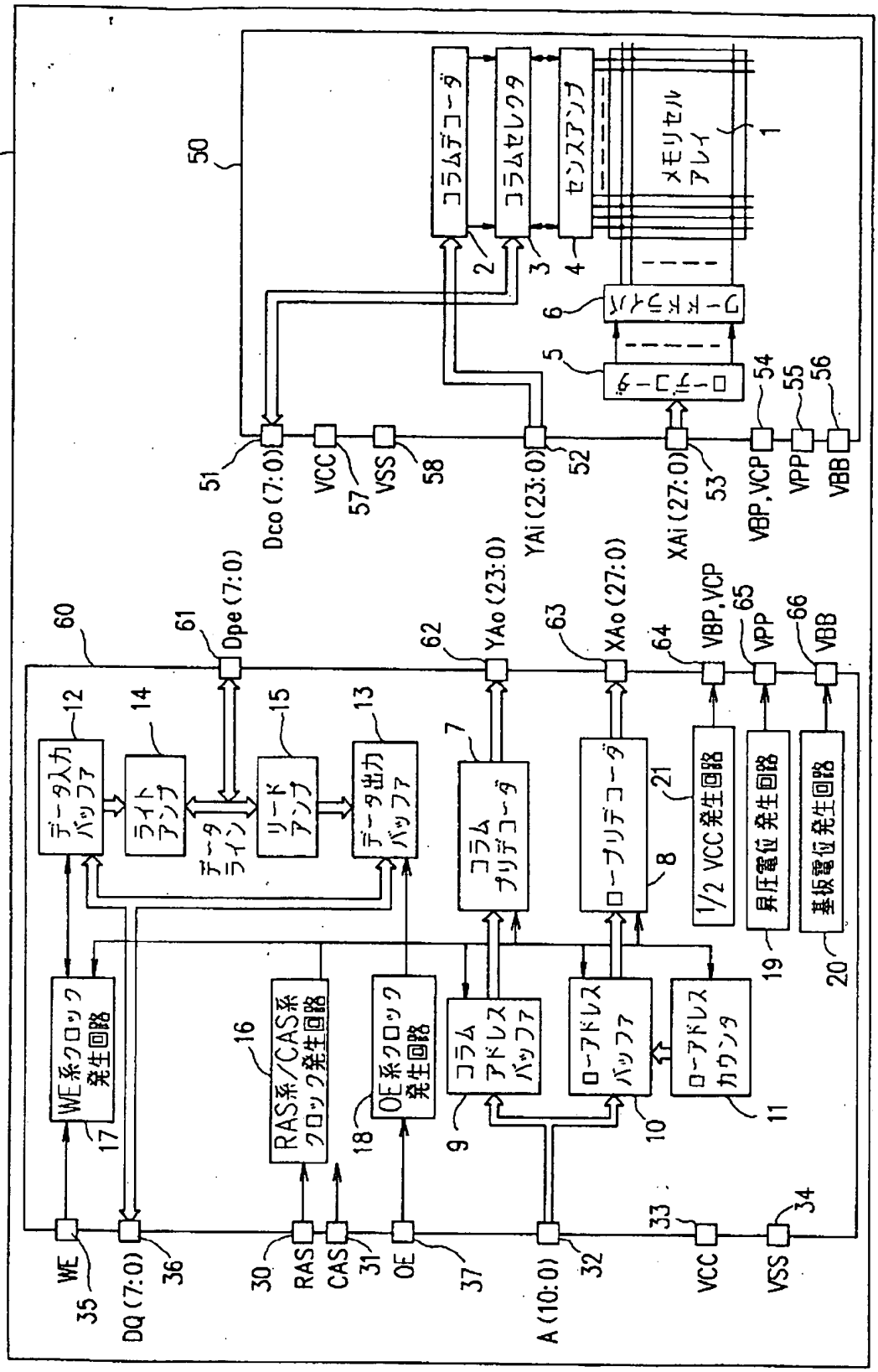
(a)


0.2
0.1
ゲート遅延 [nS]
1.5
2.0
2.5
3.0
3.5
4.0
電源電圧 [V]

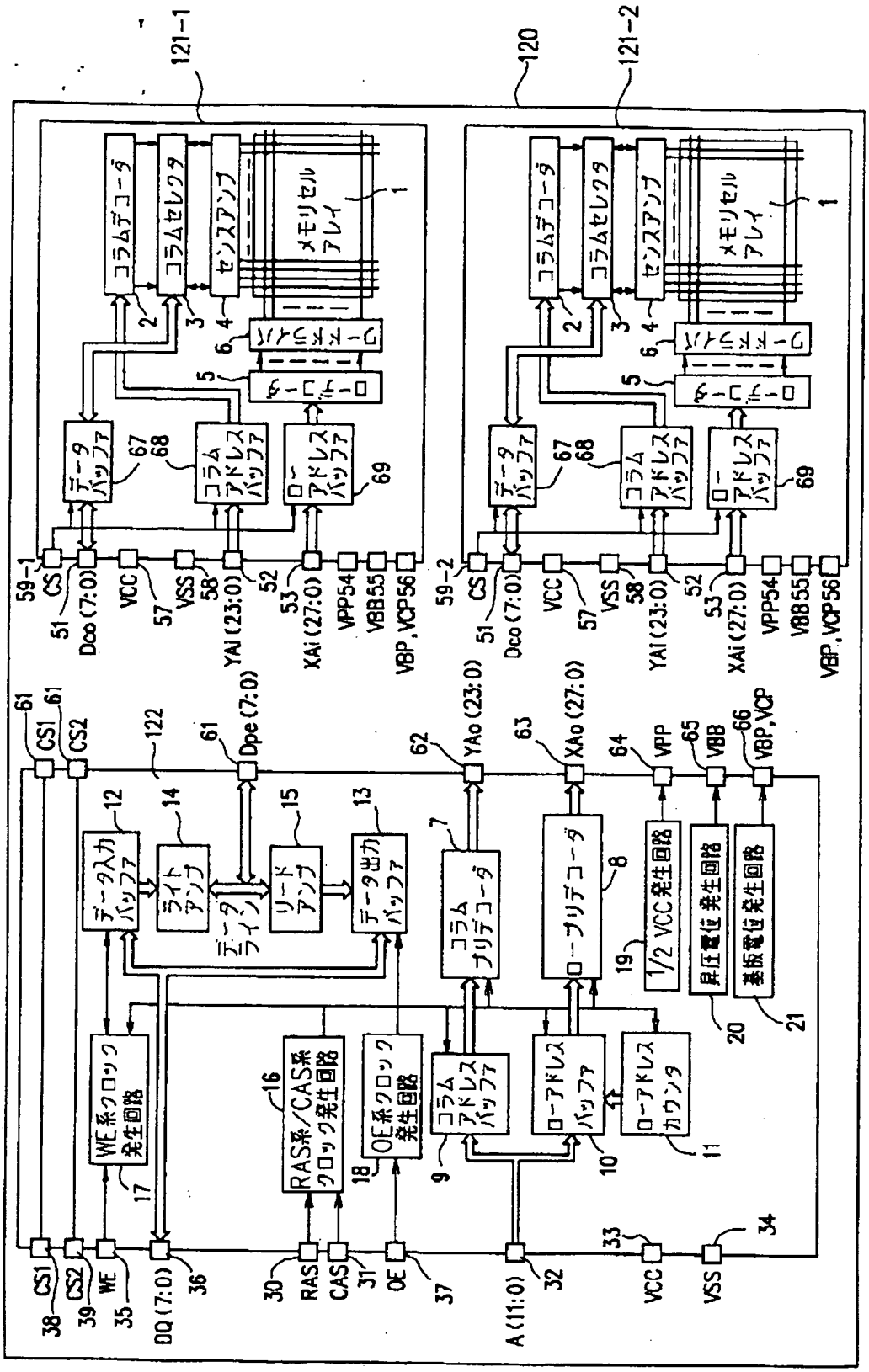
(b)


90
80
70
60
50
40
30
20
10
アクセスタイム[nS]
1.5
2.0
2.5
3.0
3.5
4.0
電源電圧 [V]

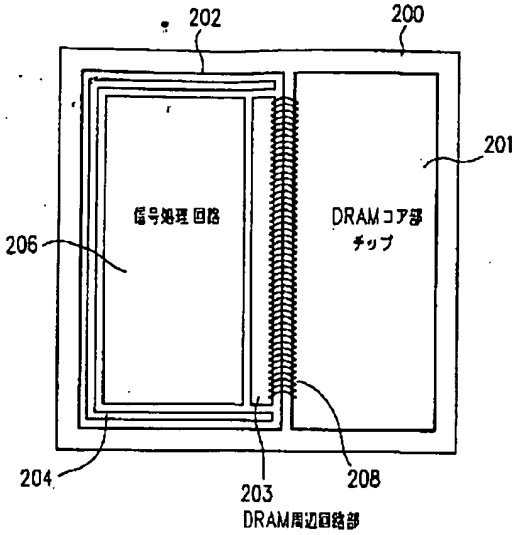
[Drawing 9]


80
50
メモリセルアレイ
1
センスアンプ
4
コラムセレクタ
3
コラムデコーダ
2
ロードライバ
5
リフレッシュカウンタ
6
51
Dco (7:0)
VCC
57
VSS
58
52
YAi (23:0)
53
XAi (27:0)
54
VBP, VCP
55
VPP
56
VBB
60
61
Dpe (7:0)
62
YAo (23:0)
63
XAo (27:0)
64
VBP, VCP
65
VPP
66
VBB
データ入力バッファ
12
ライトアンプ
14
データライン
リードアンプ
15
データ出力バッファ
13
コラムプリデコーダ
7
ロープリデコーダ
8
21
1/2 VCC発生回路
昇圧電位発生回路
基板電位発生回路
19
20
WE系クロック発生回路
17
RAS系/CAS系クロック発生回路
16
OE系クロック発生回路
18
コラムアドレスバッファ
9
ローアドレスバッファ
10
ローアドレスカウンタ
11
WE
35
DQ (7:0)
36
30
RAS
CAS
31
OE
37
A (10:0)
32
33
VCC
VSS
34

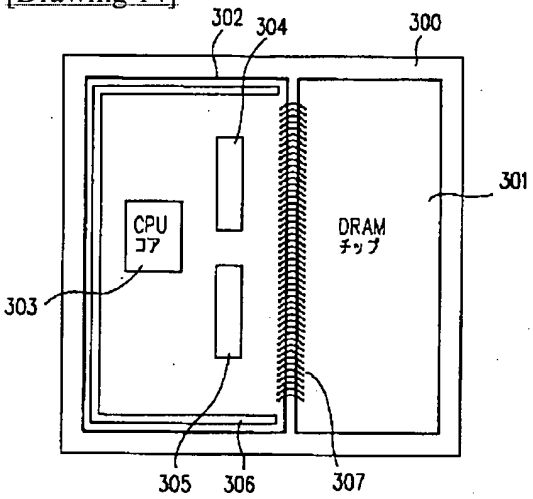
[Drawing 11]


121-1
120
121-2
メモリセルアレイ
センスアンプ
コラムセレクタ
コラムデコーダ
ロードライバ
データバッファ
コラムアドレスバッファ
ローアドレスバッファ
59-1
59-2
CS
Dco (7:0)
VCC
VSS
YAi (23:0)
XAi (27:0)
VPP54
VBB55
VBP, VCP56
Dpe (7:0)
YAo (23:0)
XAo (27:0)
VPP
VBB
VBP, VCP
CS1
CS2
データ入力バッファ
ライトアンプ
データライン
リードアンプ
データ出力バッファ
コラムプリデコーダ
ローアドレスバッファ
ローアドレスカウンタ
ローアドレスプリデコーダ
1/2 VCC発生回路
昇圧電位発生回路
基板電位発生回路
WE系クロック発生回路
RAS系/CAS系クロック発生回路
OE系クロック発生回路
WE
RAS
CAS
OE
DQ (7:0)
A (11:0)
VCC
VSS

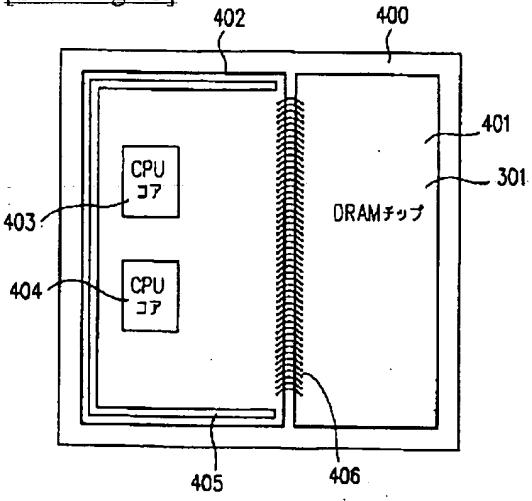
[Drawing 13]



[Drawing 14]



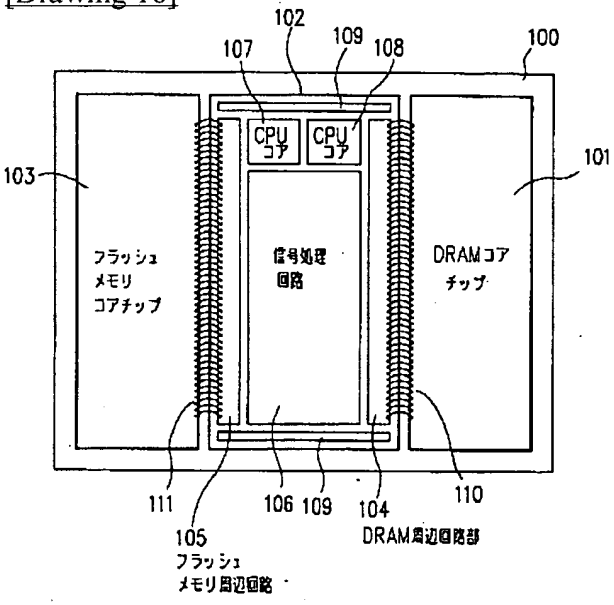
[Drawing 15]



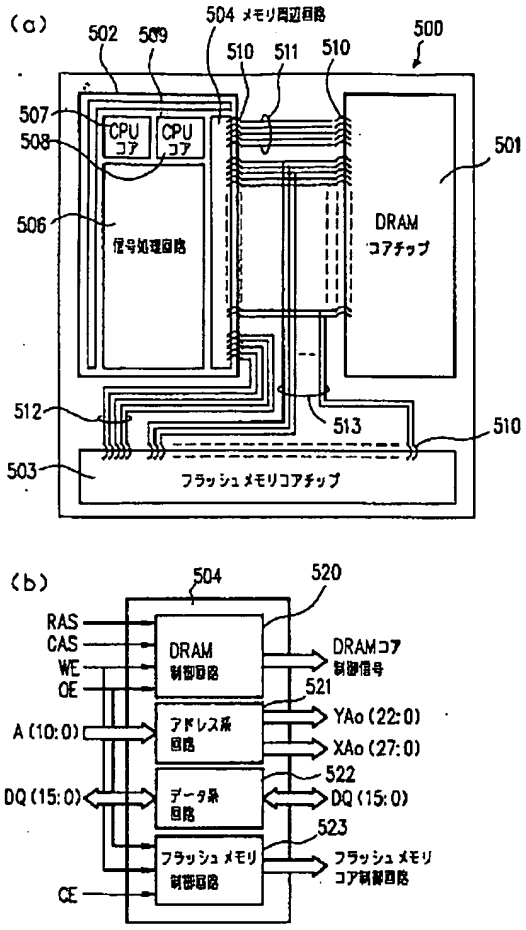
[Drawing 17]

	*システム構成1	システム構成2	システム構成3
	ディスクリート	MCM 汎用チップ	本発明
電源電圧	3.3V (1.0)	3.3V (1.0)	1.9V (0.58)
消費電力	957mW (1.0)	937mW (0.98)	244mW (0.26)
実装面積	2,770mm^2 (1.0)	1,450mm^2 (0.52)	1,110mm^2 (0.40)
チップコスト	¥4,660 (1.0)	¥4,370 (0.98)	¥4,430 (1.20)
クロック	20MHz (1.0)	20MHz (1.0)	10MHz (0.5)
システムコスト	¥16,000 (1.00)	¥16,000 (1.00)	¥14,400 (0.9)
備考	*データバス幅 8b		*データバス幅 16b *2パラレル処理

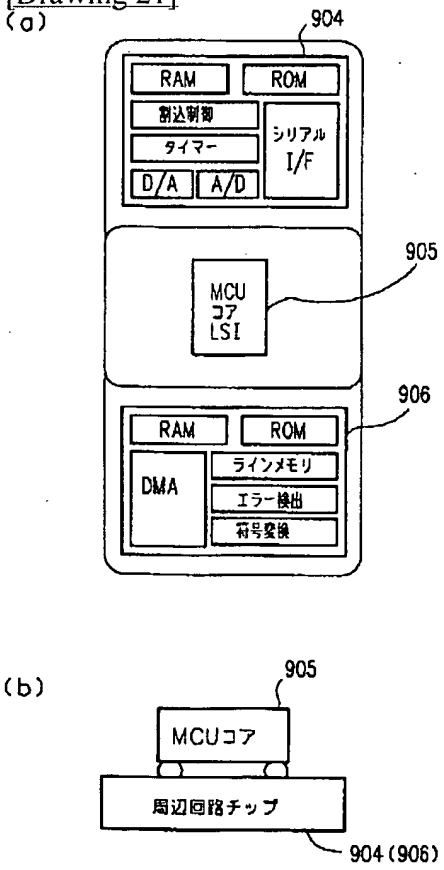
[Drawing 18]



[Drawing 19]

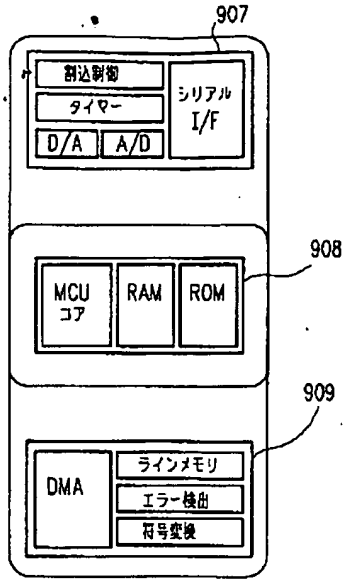


[Drawing 21]

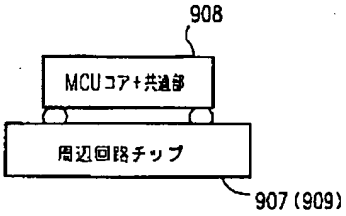


[Drawing 22]

(a)



(b)



[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the example of circuitry of DRAM conventionally.
[Drawing 2] It is the sample layout of DRAM in drawing 1 .
[Drawing 3] It is drawing showing the example of a system configuration conventionally using semiconductor memory.
[Drawing 4] (a) is drawing showing typically the layout of the semiconductor device which two or more usual circuit blocks classified functionally were shown, (b) showed typically the layout of the semiconductor device which accumulated these circuit blocks on one semiconductor chip, and (c) classified the circuit block into two groups based on a block parameter called digital one or an analog, and rearranged each on two different semiconductor chips.
[Drawing 5] (a) is [the sectional view and (c of the top view of MCM and (b))] the perspective view.
[Drawing 6] (a) And (b) is a top view explaining the 1st method of allocation two or more blocks.
[Drawing 7] (a) And (b) is a top view explaining the 2nd method of allocation two or more blocks.
[Drawing 8] It is the flow chart which shows the manufacture approach of the semiconductor device by this invention.
[Drawing 9] It is the 1st example of a configuration of the semiconductor memory in this invention.
[Drawing 10] It is the sample layout of the semiconductor memory in drawing 9 .
[Drawing 11] It is the 2nd example of a configuration of the semiconductor memory in this invention.
[Drawing 12] It is the example of mounting of the semiconductor memory in drawing 11 .
[Drawing 13] It is the 1st example of a configuration of the semiconductor device of this invention.
[Drawing 14] It is the 2nd example of a configuration of the semiconductor device of this invention.
[Drawing 15] It is the 3rd example of a configuration of the semiconductor device of this invention.
[Drawing 16] It is drawing showing the supply voltage dependence property of a logic-gate time delay and DRAM access time.
[Drawing 17] It is drawing showing many engine-performance comparisons by the example of a system configuration.
[Drawing 18] It is the 4th example of a configuration of the semiconductor device of this invention.
[Drawing 19] It is the 5th example of a configuration of the semiconductor device in this invention.
[Drawing 20] Drawing in which (a) shows the configuration of a control oriented microcomputer typically, and (b) are drawings showing the configuration of the microcomputer for image processings typically.
[Drawing 21] Drawing for (a) to explain division of a circuit block about a control oriented microcomputer and the microcomputer for image processings and (b) are the sectional views showing typically connection of two semiconductor chips with which the divided circuit block was formed.
[Drawing 22] Other drawings for (a) to explain division of a circuit block about a control oriented microcomputer and the microcomputer for image processings and (b) are the sectional views showing typically connection of two semiconductor chips with which the divided circuit block was formed.
[Description of Notations]
1 .... Memory cell array,
2 .... Column decoder,
3 .... Column selector,
4 .... Sense amplifier,
5 .... Low decoder,
6 .... WORD line driver,
7 .... Column PURIDE coder,
8 .... Low pulley decoder,
9 .... Column address buffer,
10 .... Row address buffer,

11 .... Row address counter,
12 .... Data input buffer,
13 .... Data output buffer,
14 .... Light amplifier,
15 .... Lead amplifier,
16 .... A RAS system / CAS system clock generation circuit,
17 .... WE system clock generation circuit,
18 .... OE system clock generation circuit,
19 .... Pressure-up potential generating circuit,
20 .... Substrate potential generating circuit,
21 .... 1 / 2VCC potential generating circuit,
30 .... RAS signal input terminal,
31 .... CAS signal input terminal,
32 .... Address input terminal,
33 .... VCC terminal,
35 .... WE signal input terminal,
36 .... Data input/output terminal,
37 .... OE signal input terminal,
38 .... CS1 signal input terminal,
39 .... CS2 signal input terminal,
40 .... Pad,
50 .... DRAM core section,
51 .... Data input/output terminal,
52 .... Column PURIDE coder input,
53 .... Low pulley decoder input,
54 .... VBP/VCP terminal,
55 .... VPP terminal,
56 .... VBB terminal,
57 .... VCC terminal,
60 .... DRAM circumference circuit section,
61 .... Data input/output terminal,
62 .... Column PURIDE coder output,
63 .... Low pulley decoder output,
64 .... VBP/VCP terminal,
65 .... VPP terminal,
66 .... VBB terminal,
67, 68, 69 .... Signal-line buffer,
70 .... Printed-circuit board
71 .... Signal processing LSI
72 .... DRAM,
73 .... Printed circuit
81 .... Wire bond wiring,
83 .... Pad,
94 .... DRAM circumference circuit section,
95 .... DRAM,
100 .... Substrate,
101 .... DRAM core section chip,
102 .... Signal-processing chip,
103 .... Flash memory core section chip,
104 .... DRAM circumference circuit section,
105 .... Flash memory circumference circuit section,
106 .... Digital disposal circuit,
107 108 .... Core based CPU
109 .... Pad,
110 111 .... Wire bond wiring,
120 .... Substrate,

122 .... Memory circumference circuit section chip,
131 .... Substrate wiring,
200 .... Substrate,
201 .... DRAM core section chip,
202 .... Signal-processing chip,
203 .... DRAM circumference circuit section,
204 .... Pad,
300 .... Substrate,
301 .... DRAM chip,
302 .... Signal-processing chip,
303 .... Core based CPU
304 .... Data cache,
305 .... Instruction cache,
306 .... Pad,
307 .... Wire bond wiring,
400 .... Substrate,
401 .... DRAM chip,
402 .... Signal-processing chip,
403 404 .... Core based CPU
405 .... Pad,
406 .... Wire bond wiring,
500 .... Substrate,
501 .... DRAM core section chip,
502 .... Signal-processing chip,
503 .... Flash memory core section chip,
504 .... Memory circumference circuit section,
506 .... Digital disposal circuit,
507 508 .... Core based CPU
510 .... Wire bond wiring,
511, 512, 513 .... Substrate wiring,
520 .... DRAM control circuit,
521 .... Address system circuit,
522 .... Data system circuit,
523 .... Flash memory control circuit.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which fitted the multi chip module (it is hereafter described as MCM) especially about a semiconductor device and its manufacture approaches, such as semiconductor memory equipment.
[0002]
[Description of the Prior Art] The dynamic random access memory (DRAM) which is one of the semiconductor memory is equipped with the memory cell array by which the memory cell has been arranged in the shape of an array as the storage section. The chip is realized by circuitry as shown to drawing 1 that DRAM can lessen the number of pins of a package as much as possible. In drawing 1 , DRAM95 as circuit block 50 arranged in the same pitch as the memory cell in the memory cell array 1 focusing on the memory cell array 1 by which the memory cell has been arranged in the shape of an array the column selector 3 which chooses the bit data of the location of arbitration from the signals amplified by the sense amplifier 4 for amplifying the signal of the low decoder 5 for choosing a WORD line and the WORD line driver 6, and the bit line, and the sense amplifier 4, and is outputted to a data line -- and It has the column decoder 2 which generates the selection signal given to the column selector 3, and the circuit block 50 with which the circuit arranged in the same pitch as the memory cell in the memory cell array 1 and the memory cell array 1 was doubled is expressed as the memory core section in subsequent explanation. moreover, as a circuit arranged without being dependent on the memory cell pitch in the memory cell array 1 A row address from the address signal input terminal A(10:0) 32 The row address buffer 10 to receive and the column address In order to change into the signal given to the low decoder 5 and the column decoder 2 from the output signal of the column address buffer 9 to receive, the row address counter 11 which generates a refresh address, the row address buffer 10, and the column address buffer 9 The address signal inputted The data writing to the data input buffer 12 which outputs and inputs the data to the low pulley decoder 8 decoded beforehand and the column PURIDE coder 7, and the data input/output terminal DQ(7:0) 36 and the data output buffer 13, and a memory cell Based on RAS and the CAS signal which are inputted from the lead amplifier 15, the RAS signal input terminal 30, and the CAS signal input terminal 31 for performing data read-out from the light amplifier 14 for carrying out, and a memory cell, the timing signal inside DRAM OE signal inputted from the RAS system / CAS system clock generation circuit 16 to generate, WE system clock generation circuit 17 which generates the timing signal of writing based on WE signal inputted from WE signal input terminal 35, and OE signal input terminal 37 As OE system clock generation circuit 18 which generates the timing signal of data output on a radical, and a circuit which generates an electrical potential difference required for the interior of DRAM It has the pressure-up potential generating circuit 19 which is needed for carrying out the pressure up of the word line potential, the substrate potential generating circuit 20 which generates the potential which gives a substrate, and the 1 / 2VCC generating circuit 21 which is needed as potential given to bit line precharge and a cel plate. In subsequent explanation, the circuit arranged without depending is doubled and it is expressed as the memory cell pitch in this MORISERU array 1 with the memory circumference circuit section.
[0003] By having the circuit shown in drawing 1 on 1 chip, DRAM95 serves as only the address, data, several control signal pins, and power-source pins as an external pin in the case of mounting in a package, and can be mounted with a small package. If 16MDRAMs of 8 bit-data I/O are taken for an example, two pins are used as four pins and a power-source pin as eight pins and a control signal pin as 11 pins and a data I/O pin as an address pin, and as the number of need pins, it is 25 pins, and can mount in the package of 28 pins.
[0004] The chip sample layout of DRAM of the circuitry shown by drawing 1 is shown in drawing 2 . In drawing 2 , the case of 16 M bit DRAM is shown, the memory cell array 1 is quadrisected by the 4M bit plate, and 16 ****s of each 4M bit plate are carried out to the pan at the memory cell block 96 of 256K bits. Each memory cell block 96 of 256K bits is equipped with the memory cell of 256 low x1024 column, and, as for the sense amplifier 4 and the column

selector 3, the number of columns and the 1024 same numbers of a memory cell are arranged at each memory cell block. The low decoder 6 and the WORD driver 5 are arranged for every memory cell block, the column decoder 2 is arranged for every plate, and the memory circumference circuit section is arranged at 94 between the column decoders 2 of right and left in a chip center section, and a chip periphery. Although the selection signal to the column selector 3 which is the output of the column decoder 2 is a common signal to a plate on either side here, the column decoder 2 is arranged at the plate on either side, respectively, because a selection-signal line cannot cross the memory circumference circuit section 94 of a center section. The pad for making connection with an external pin is arranged in the pad formation section 40 in the chip center section 94, and has connected this pad and the external pin of a package with wire bond.

[0005] Here, each signal terminals 30-32 in the case where it mounts in a package, and the terminal capacity of 35-37 have the largest data input/output terminal 36 used as an input/output terminal, it becomes the sum total of the gate capacitance of an input transistor, the wiring capacity from a terminal to an input transistor, the capacity of the surge protection device for input transistors, the diffusion capacitance of a signal output transistor, the capacity of the surge protection device for output transistors, and the lead of a package and wire bond capacity, and about 5pF exists. Generally two or more memory is used for a system, and each terminal of two or more memory is connected in common by bus wiring. For this reason, in DRAM, characterization is performed as that by which 50pF load-carrying capacity is connected to each pin, and the about 8-16-bit thing is realized in the present condition as bit width of face of data I/O in consideration of increase of the power consumption not only by a limit of the number of package pins but load-carrying capacity drive, and a noise etc.

[0006] The example of a system implementation means which used DRAM for drawing 3 is shown. 70 is a printed-circuit board and signal processing LSI 71, such as DRAM72, CPU, etc. which were packed on this printed-circuit board 70, is carried out with the pewter. The printed circuit 73 connects between DRAM72 and signal processing LSI 71. Although the example of a system configuration using one DRAM was shown in drawing 3 , there are also many systems using DRAM two or more.

[0007]

[Problem(s) to be Solved by the Invention] In order to realize a memory cell capacitor mass in small area, and a memory cell transistor with little leakage current, DRAM uses a complicated semi-conductor manufacture process with many routing counters, is manufactured, and it is about 1.5 times the manufacturing cost of this compared with the logic LSI process of realizing logic LSI in the same design rule in the DRAM process using a 0.5-micrometer design rule.

[0008] In the DRAM circuitry shown in drawing 1 , the part which needs a DRAM process is only the memory cell array 1, and parts other than memory cell array 1 on a chip can be manufactured in the logic LSI process of realizing logic LSI. However, as shown in drawing 2 , all the parts of the circuitry shown in drawing 1 are manufactured in the DRAM process, and DRAM is made expensive.

[0009] This is the same also in semiconductor memory other than DRAM, has realized that in which SRAM, EEPROM, the flash memory, etc. included the circumference circuit sections other than a memory cell array in the expensive process compared with the logic LSI process on 1 chip, and makes semiconductor memory expensive.

[0010] Moreover, as mentioned above, only the thing to 8-16 bits was realized, but the bit width of face of data I/O of memory had realized multi-bit width-of-face data I/O in the system which needs the data transfer of multi-bit width of face using much memory of small capacity, and had become a large area and an expensive system.

[0011] Furthermore, although development of the MCM technique aiming at mounting two or more bare chips containing memory in the same substrate with a miniaturization and improvement in the speed of a system, and connecting between chips with the shortest wiring prospers Since the expensive memory manufactured with the configuration of conventional drawing 2 also in the memory chip used for this MCM is used as it is and the data I/O bit width of face in memory 1 chip is restricted, In order to realize data I/O of multi-bit width of face, much memory of small capacity needed to be used.

[0012] Moreover, for improvement in the speed of the stored data maintenance property of a memory cell, or access time, in DRAM, the semi-conductor substrate is set as negative potential, and this negative potential is generated by the substrate potential generating circuit 20 accumulated by the DRAM chip. On the other hand, since it becomes the configuration that a semi-conductor substrate is grounded, compared with Logic LSI, the impedance of the semi-conductor substrate of DRAM will become high, and, as for Logic LSI, a latch rise and surge resistance will usually become low. For this reason, while needing input surge protection of a large area, in DRAM using a detailed-ized process technique, 3-fold well structure process which makes the substrate of only a memory cell field negative potential is needed, and DRAM is made more expensive.

[0013] Furthermore, in the system using memory, using two or more kinds of memory, such as not only DRAM but SRAM, EEPROM, a flash memory, etc., in many cases, all of such memory will carry the circumference circuit on the

same chip as a memory cell, and all memory chips will have the circuit which carries out same actuation.
[0014] This invention is made in view of the above-mentioned situation, and the place made into the purpose of this invention is to offer a semiconductor device with a high function by the low price.
[0015]
[Means for Solving the Problem] The semiconductor device of this invention is a semiconductor device equipped with two or more circuit blocks including the 1st circuit block and the 2nd circuit block with which block parameters differ, this 1st circuit block is formed on the 1st semiconductor chip, this 2nd circuit block is formed on the 2nd semiconductor chip, moreover it connects with this 1st circuit block electrically, and the above-mentioned purpose is attained by that.
[0016] Said block parameter is a parameter chosen from the group which consists of a difference of a clock frequency of operation, the design Ruhr, the threshold (Vt) of a transistor, supply voltage, a digital circuit, or an analog circuit, the difference of a usual MOS circuit or a usual CMOS circuit, a bipolar circuit, or the Bayh CMOS circuit, a difference of ROM or RAM, and a difference of logic or memory.
[0017] Said 1st circuit block may be a memory cell block which has two or more memory cells, and said 2nd circuit block may be a memory circumference circuit block for accessing the memory cell as which this memory cell block was chosen.
[0018] Said 1st circuit block may be a core based CPU, and said 2nd circuit block may be a circumference circuit block.
[0019] The process which divides the circuit where the manufacture approach of the semiconductor device of this invention may be accumulated on one semiconductor chip into the 1st circuit block and the 2nd circuit block with which block parameters differ, The process which connects electrically the process which forms this 1st circuit block on the 1st semiconductor chip, the process which forms this 2nd circuit block on the 2nd semiconductor chip, and this 1st circuit block and this 2nd circuit block is included, and the above-mentioned purpose is attained by that.
[0020] Said block parameter is a parameter chosen from the group which consists of a difference of a clock frequency of operation, the design Ruhr, the threshold (Vt) of a transistor, supply voltage, a digital circuit, or an analog circuit, the difference of a usual MOS circuit or a usual CMOS circuit, a bipolar circuit, or the Bayh CMOS circuit, a difference of ROM or RAM, and a difference of logic or memory.
[0021] Said 1st circuit block may be a memory cell block which has two or more memory cells, and said 2nd circuit block may be a memory circumference circuit block for accessing the memory cell as which this memory cell block was chosen.
[0022] Said 1st circuit block may be a core based CPU, and said 2nd circuit block may be a circumference circuit block.
[0023] The circuit which may be accumulated on one semiconductor chip other semiconductor devices of this invention It is the semiconductor device divided into the 1st circuit block and the 2nd circuit block with which block parameters differ. This 1st circuit block is formed on the 1st semiconductor chip, this 2nd circuit block is formed on the 2nd semiconductor chip, this 1st circuit block and this 2nd circuit block are connected electrically, and the above-mentioned purpose is attained by that.
[0024] Said block parameter is a parameter chosen from the group which consists of a difference of a clock frequency of operation, the design Ruhr, the threshold (Vt) of a transistor, supply voltage, a digital circuit, or an analog circuit, the difference of a usual MOS circuit or a usual CMOS circuit, a bipolar circuit, or the Bayh CMOS circuit, a difference of ROM or RAM, and a difference of logic or memory.
[0025] The 1st circuit section which has two or more circuit blocks for the semiconductor device of further others of this invention to achieve the 1st function at least, This 1st function is the semiconductor device equipped with the 2nd circuit section which has the circuit block for achieving the 2nd different function. At least one circuit block among the circuit blocks of this plurality of this 1st circuit section With the circuit block of this 2nd circuit section, it is formed on the 1st semiconductor chip. The remaining circuit block of this 1st circuit section It is formed on the 2nd different semiconductor chip from this 1st semiconductor chip. It connects with the circuit block formed on the 2nd semiconductor chip electrically. and -- this -- The block parameter about the circuit block of this 1st circuit section formed on this 1st semiconductor chip Rather than the block parameter about other circuit blocks of this 1st circuit section formed on this 2nd semiconductor chip, the above-mentioned purpose is attained by near and its thing by the block parameter about the circuit block of this 2nd circuit section.
[0026] Said 1st circuit section has the memory cell block and the memory circumference circuit block at least as two or more circuit blocks which achieve said 1st function. Said 2nd circuit section As a circuit block which achieves said 2nd function, it has the digital disposal circuit, this digital disposal circuit and this memory circumference circuit block may be formed on said 1st semiconductor chip, and this memory cell block may be formed on said 2nd semiconductor chip.
[0027] Said block parameter is a parameter chosen from the group which consists of a difference of a clock frequency

of operation, the design Ruhr, the threshold (Vt) of a transistor, supply voltage, a digital circuit, or an analog circuit, the difference of a usual MOS circuit or a usual CMOS circuit, a bipolar circuit, or the Bayh CMOS circuit, a difference of ROM or RAM, and a difference of logic or memory.

[0028] The memory cell of these memory cell arrays in this semiconductor memory core chip is specified as an input/output terminal for the memory circumference circuit section chip of this invention to transmit and receive a signal to other semiconductor memory core chips containing a memory cell array with the address given, it has the memory circumference circuit which performs data read-out or the writing to this memory cell, and the above-mentioned purpose is attained by that.

[0029] The memory core chip of this invention is equipped with the input/output terminal and memory cell array for transmitting and receiving a signal to other semiconductor chips including a memory circumference circuit, with the address given, a memory cell is specified from this memory circumference circuit of this semiconductor chip, data read-out or the writing to this memory cell is performed, and the above-mentioned purpose is attained by that.

[0030] at least one memory core section chip with which the semiconductor-memory equipment of this invention is formed using the 1st semi-conductor manufacture process -- this -- it has a means connect the memory circumference circuit section chip formed using the 2nd different semi-conductor manufacture process from the 1st semi-conductor manufacture process, and this memory core section chip and this memory circumference circuit section chip, and the above-mentioned purpose is attained by that.

[0031] Including a memory cell for said memory core section chip to memorize data, said memory circumference circuit section chip may specify this memory cell in this memory core section chip with the address given, and may perform data read-out or the writing to this memory cell.

[0032] Two or more memory core section chips with which other semiconductor memory equipments of this invention are formed using the 1st semi-conductor manufacture process, this -- with the memory circumference circuit section chip formed using the 2nd different semi-conductor manufacture process from the 1st semi-conductor manufacture process It has a means to connect these two or more memory core section chips and this memory circumference circuit section chip, and said memory core section chip shares some [at least] circuits in this memory circumference circuit chip, and the above-mentioned purpose is attained by that.

[0033] At least one memory core section chip containing a memory cell for the semiconductor device of further others of this invention to memorize the data formed using the 1st semi-conductor manufacture process, this -- with the signal-processing chip which carries the digital disposal circuit which processes using the data memorized by the memory circumference circuit section and the memory core section chip which are formed using the 2nd different semi-conductor manufacture process from the 1st semi-conductor manufacture process It has a means to connect this memory core section chip and this signal-processing chip, and the above-mentioned purpose is attained by that.

[0034] With the address given, said memory circumference circuit section may specify said memory cell in said memory core section chip, and may perform data read-out or the writing to this memory cell.

[0035] Said memory core section chip has more than one, and shares some [at least] circuits in a memory circumference circuit chip.

[0036] The semiconductor device of further others of this invention is a semiconductor device in which the memory chip and the signal-processing chip were mounted by the multichip mounting means. This memory chip The memory cell array section equipped with two or more memory cells which store data, An access means to specify this memory cell in this memory cell array with the address given, and to output and input data, It has the data terminal for outputting and inputting two or more data to juxtaposition. This signal-processing chip It has the data terminal which outputs and inputs two or more data to juxtaposition, and has a means to transmit two or more data to juxtaposition between this memory chip and this signal-processing chip, and the above-mentioned purpose is attained by that.

[0037] said memory chip is realized using the 1st semi-conductor manufacture process -- having -- **** -- said signal-processing chip -- this -- you may realize using the 2nd different semi-conductor manufacture process from the 1st semi-conductor manufacture process.

[0038] Said signal-processing chip may be equipped with further two or more digital disposal circuits.

[0039] The semiconductor device of further others of this invention is a semiconductor device in which the memory core section chip and the signal-processing chip were mounted by the multichip mounting means. This memory core section chip It has the memory cell array equipped with two or more memory cells which store data, and the data terminal which output and input two or more data to juxtaposition. This signal-processing chip This memory cell in this memory core section chip is specified with the address given. Performed data read-out or the writing to this memory cell, and it has the data terminal and two or more digital disposal circuits which output and input two or more data to juxtaposition. It has a means to transmit two or more data between this memory core section chip and these signal-processing chips to juxtaposition, and the above-mentioned purpose is attained by that.

[0040] said memory core section chip is realized using the 1st semi-conductor manufacture process -- having -- **** --

said signal-processing chip -- this -- it may be formed using the 2nd different semi-conductor manufacture process from the 1st semi-conductor manufacture process.

[0041]

[Embodiment of the Invention] The semiconductor device of this invention is equipped with two or more circuit blocks including the 1st circuit block and the 2nd circuit block with which block parameters differ, the 1st circuit block is formed on the 1st semiconductor chip, and the 2nd circuit block is formed on the 2nd semiconductor chip. Here, a block parameter is the difference of a difference of a clock frequency of operation, the design Ruhr, the threshold (Vt) of a transistor, supply voltage, a digital circuit, or an analog circuit, a MOS circuit, a usual CMOS circuit or a usual bipolar circuit, the Bayh CMOS circuit, etc. As a block parameter, a difference of logic properties, such as a difference of ROM or RAM and a difference of logic or memory, is also included in others.

[0042] A large-scale system is formed on one semiconductor chip in recent years, by it, properties, such as a working speed, are raised and the view of the system-on-chip which is going to reduce a manufacturing cost is becoming in use. In the semiconductor device of such a system-on-chip mold, two or more circuit blocks are accumulated on one semiconductor chip, and the design is performed so that the circuit block of these plurality may be arranged with the optimal layout. It has been believed that being accumulated on one semiconductor chip is most desirable as for two or more circuit blocks accumulated although block parameters may differ mutually. An invention-in-this-application person dared classify two or more circuit blocks regardless of the common sense based on various parameters, and when distributing on a different semiconductor chip, he found out that effectiveness, such as reduction of a manufacturing cost, was acquired on the contrary.

[0043] It is whether to form an important point on each semiconductor chip on the occasion of allocation of two or more circuit blocks by classifying each circuit block according to what kind of criteria. The point is explained below, referring to drawing 4 (a) - (c).

[0044] Drawing 4 (a) shows two or more usual circuit blocks classified functionally, and drawing 4 (b) shows typically the layout of the semiconductor device which accumulated these circuit blocks on one semiconductor chip. Drawing 4 (c) classifies a circuit block into two groups based on a block parameter called digital one or an analog, and shows typically the layout of the semiconductor device which rearranged each on two different semiconductor chips.

[0045] The image processing system used for a home video game machine etc. consists of a CPU, LSI for image processings, and an NTSC encoder, as shown in drawing 4 (a). The NTSC encoder contains the logical circuit (LOGIC) section and the D/A converter (DAC) section, and as a whole, these operate so that the function of an NTSC encoder may be demonstrated. The LOGIC section controls the output level of the DAC section based on a RGB digital signal. The DAC section contains the decoder part (DAC-DEC) which decodes a digital signal, and the current cel array part (DAC-ARRAY) which outputs an analog signal according to the signal from a decoder part. A decoder part (DAC-DEC) is constituted by the digital circuit, and the current cel array part (DAC-ARRAY) is constituted by the analog circuit. Consequently, an NTSC encoder can generate an NTSC composite signal from a RGB digital signal. CPU, LSI for image processings, and an NTSC encoder are respectively formed on a separate semiconductor chip. Each semiconductor chip is arranged on the circuit board, and is electrically connected by wiring on the circuit board. Since it is thought that interconnecting with wiring on the circuit board checks high-speed operation, the system of drawing 4 (a) is being accumulated by development of a large-scale LSI manufacturing technology, and fullness of the design exchange tool using CAD on one semiconductor chip, as shown in drawing 4 (b).

[0046] According to the invention in this application, based on a block parameter called digital one or an analog, the circuit block of the above-mentioned system is classified and is distributed on a different semiconductor chip. The circuit part which performs digital actuation in the LOGIC section in an NTSC encoder and the DAC section is specifically separated from the circuit part which performs analog actuation in the DAC section, and it is accumulated on one semiconductor chip (for digital circuits) with a CPU block and CG block. On the other hand, the analog circuit part of the DAC section of an NTSC encoder is formed on other semiconductor chips (for analog circuits). The following effectiveness is acquired by doing in this way. That is, the analog circuit part of the DAC section of an NTSC encoder is sensitive to a noise, and tends to receive the bad influence by the noise. For this reason, if the DAC section is formed on the same semiconductor chip as the LOGIC section currently formed of the digital circuit, there is a possibility that the noise resulting from actuation of a digital circuit may reach the DAC section through a semiconductor chip. If a circuit block required in order to attain the function which an NTSC encoder has is formed on two semiconductor chips as mentioned above, the problem by such noise is solvable. Moreover, according to a semi-conductor manufacture process, it differs and each design rule also differs from the process which forms an analog circuit, and the process which forms a digital circuit. For this reason, if it divides into the semiconductor chip for digital circuits, and the semiconductor chip for analog circuits and a production process is performed, it is the optimal design rule about each semiconductor chip, and can produce in the manufacture procedure which moreover omitted the unnecessary process. Usually, since the cost per process is relatively expensive, if the severe process of a design rule

finds a producible circuit block according to a loose design rule and separates the circuit block on other semiconductor chips, a manufacturing cost can be reduced as a whole.

[0047] Thus, after separating into two or more semiconductor chips and forming a circuit block, MCM is formed from the semiconductor chip of these plurality. MCM arranges two LSI chips, as shown for example, in drawing 5 (a) - (c), and it is produced by interconnecting by the solder bump. The semiconductor device of this invention does not form one module, combining two or more existing semiconductor chips simply, but after the point that the semiconductor device of this invention differs from the conventional MCM builds one system which has two or more circuit blocks, a specific block parameter is in the point which uses for a module the semiconductor chip separated for every group common to mutual, or near group of a block parameter.

[0048] With other operation gestalten, the memory cell block which has two or more memory cells, and the memory circumference circuit block for accessing the memory cell as which it was chosen under memory cell block are formed on a different semiconductor chip. With a memory cell block and a memory circumference circuit block, design rules (lower limit) differ and the sequences of a manufacture process also differ. However, it was believed that these blocks should have been accumulated on one semiconductor chip in order to demonstrate the function as a DRAM. According to this invention, a memory cell block and a circumference circuit block are classified on the basis of a block parameter called a design rule, and are formed on a different semiconductor chip. About this invention, an example is later explained to a detail.

[0049] With other desirable operation gestalten, a core based CPU and a circumference circuit block are formed on a separate semiconductor chip. In addition, a core based CPU decodes an instruction at least, has the control section which performs control action, and the operation part which performs arithmetic logical operation, and is a circuit which controls a peripheral device here.

[0050] It roughly divides into the method of allocation a block of these plurality, and there are two in it. As the circuit block with which a block parameter differs from other circuit blocks is found out when C is formed on one semiconductor chip 700 from two or more circuit blocks A for attaining one function, as shown in drawing 6 (a), and shown in drawing 6 (b), the 1st forms Blocks A and B on a semiconductor chip 710, and forms Block C on a semiconductor chip 720. The two semiconductor chips 710 and 720 are connected mutually.

[0051] As the 2nd is shown in drawing 7 (a), two or more circuit block A-C for attaining the 1st function is formed on the 1st semiconductor chip 800. And when two or more circuit blocks D and E for attaining the 2nd function are formed on the 2nd semiconductor chip 810, it sets. As shown in drawing 7 (b), the circuit block C with which a block parameter differs from other circuit blocks A and B is found out, and it forms on other semiconductor chips 830. The remaining circuit blocks A and B are formed on a semiconductor chip 820. The two semiconductor chips 820 and 830 are connected mutually.

[0052] Below, the manufacture approach of the semiconductor device by this invention is explained, referring to drawing 8 .

[0053] First, at the process S1 shown in drawing 8 , a netlist is determined using CAD and a block parameter is read. Then, hierarchy expansion is performed about a circuit block. Next, the group division of the circuit block is carried out on the basis of a specific block parameter at a process S2. Then, a group hierarchy is added to a netlist at a process S3. By this, assignment is completed on the semiconductor chip of the plurality of a circuit block.

[0054] The well-known process for manufacturing each semiconductor chip after this will be performed. It is process S4, and the layout of the circuit formed on each semiconductor chip is determined, and, specifically, a layout is verified at a process S5. Mask data are produced at a process S6, and a mask is produced at a process S7. A circuit is formed in each semiconductor chip by the process S8 and S9 using those masks. A process S8 and S9 include two or more sub processes, such as thin film deposition and a photolithography, respectively.

[0055] In this way, preferably, with an MCM technique, it connects mutually and at least two formed semiconductor chips form one semiconductor device.

[0056] Next, if a circuit block is divided based on what kind of block parameter, it will explain using the following table what kind of advantage is acquired. Table 5 has indicated the circuit name formed on the 2nd semiconductor chip at the B column in the circuit name formed on the 1st semiconductor chip at the A column in the block parameter chosen as criteria of circuit block division in the C column from Table 1.

[0057]

[Table 1]

パラメータ： デザインルール

	LSI 1	LSI 2
1	周辺回路	メモリコア
2	ディジタル回路	アナログ回路
3	高速回路	低速回路
4	CMOS	バイポーラ
5	ユーザ回路	MCUコア
6	テスト回路	非テスト回路

[0058]
[Table 2]
パラメータ： 閾値（Vt）

	LSI 1	LSI 2
1	高速回路	低速回路
2	周辺回路	メモリコア
3	ディジタル	アナログ

[0059]
[Table 3]
パラメータ： 電源電圧

	LSI 1	LSI 2
1	周辺回路	メモリコア
2	ユーザ回路	MCUコア
3	ディジタル	アナログ
4	ユーザ回路	MCUコア

[0060]
[Table 4]

パラメータ： 動作周波数

	LSI 1	LSI 2
1	ユーザ回路	MCUコア
2	メモリ	MCUコア
3	高速回路	低速回路
4	テスト回路	非テスト回路

[0061]
[Table 5]
パラメータ： 論理回路・特徴

	LSI 1	LSI 2
1	ユーザ回路	MCUコア
2	演算器（FPU）	MCUコア
3	メモリ	MCUコア
4	ユーザ回路	演算器（FPU）
5	ユーザ回路	メモリ
6	ディジタル	アナログ
7	CMOS	バイポーラ
8	テスト回路	非テスト回路

[0062] The case where the 1st line of Table 1 formed circumference circuits, such as a line decoder and a train decoder, on the 1st semiconductor chip on the basis of the design rule, and the memory core circuit where many memory cells were arranged on the 2nd semiconductor chip is formed is shown. These semiconductor chips interconnect and constitute one semiconductor memory equipment.
[0063] According to the example shown in Table 1, a manufacturing cost can be reduced. If the circuit block with which design rules differ is formed on one semiconductor chip, it will be formed with the severe circuit block of a design rule to the circuit block of a design rule loose in comparison.
[0064] A production process special for formation of structure with an expensive manufacturing installation detailed required is relatively required of manufacture of a severe circuit block of a design rule too much in many cases. Relatively [a design rule], if a loose circuit block is relatively divided and formed on a semiconductor chip different from a severe circuit block, the semiconductor chip will be simply formed at a process cheap in comparison, and its manufacture yield will also improve. Consequently, the semiconductor device formed from two semiconductor chips is also manufactured with the sufficient yield at low cost as a whole.
[0065] According to the example shown in Table 2, the semiconductor device which carries out high-speed operation

by low power consumption is obtained. Generally, since the semiconductor device in which high-speed operation is possible tends to produce big leakage current, it has the inclination for power consumption to be large. Although the circuit block with the low threshold of a transistor operates at a high rate relatively, its leakage current is relatively large. if it separates into the circuit block which should be operated relatively at high speed, and the circuit block which may be operated relatively at a low speed based on the threshold of a transistor, since each semiconductor chip can be formed according to the manufacture process for which was resembled, respectively and it was suitable, by low power consumption, the semiconductor device which carries out high-speed operation is comparatively alike, and can form cheaply.

[0066] According to the example which Table 3 shows, since the optimal supply voltage can be set up for every semiconductor chip, the semiconductor device which carries out high-speed operation by low power consumption can form cheaply in comparison like the example of Table 2. Generally, the working speed of a very large-scale integrated circuit (LSI) is proportional to supply voltage. That is, if supply voltage falls, the highest frequency which can operate will become low. On the other hand, power consumption is proportional to the square of supply voltage. In the case of LSI which operates on the same frequency, the power consumption at the time of making it operate with the supply voltage of 3 volts turns into about 40% of the power consumption in the case of making it operate with the supply voltage of 5 volts. By 3 volts, when MCU for image processings which uses the MCU core (my koro controller unit core) in which 25MHz actuation is possible, for example, performs 25MHz actuation by 3 volts is formed by 50MHz actuation and 2 volts, this MCU for image processings will operate with the comparatively high supply voltage of that clock frequency. This causes consumption of useless power. In actuation of MCU, the supply voltage of 2 volts may be desirable, and the supply voltage of 3 volts may be desirable in actuation of a circumference circuit. In such a case, a MCU core and a circumference circuit are formed on a separate semiconductor chip, and if a different electrical potential difference is supplied to each semiconductor chip, as a semiconductor device, actuation of a high-speed low power will be realized under the optimal supply voltage.

[0067] According to the example shown in Table 4, a manufacturing cost can be reduced. Since it has the structure which should be manufactured according to a different manufacture process from the circuit block which operates with low clock frequency relatively [block / which operates with high clock frequency relatively / circuit], if each circuit block is formed on a separate semiconductor chip, a manufacturing cost will be reduced as a whole. Moreover, the effectiveness acquired from the example shown in Table 2 is acquired similarly.

[0068] According to the example shown in the 5th line from the 1st line of Table 5, a manufacturing cost also including design cost is reduced. In the example of the 1st line to the 5th line of Table 5, the circuit on one semiconductor chip is constituted from a circuit block with a general-purpose function between two semiconductor chips, and the configuration of the circuit on the semiconductor chip of another side is enabled to differ for every user. For this reason, although it is designed, and the semiconductor chip with which designs may differ for every user is manufactured and becomes things so that it may have various configurations, a general-purpose semiconductor chip may be used in common to the semiconductor chip of the varieties manufactured by making it such. For this reason, when manufacturing two or more semiconductor devices, or when a design change is performed, the advantage that a manufacturing cost is reduced is acquired.

[0069] According to the example shown in the 6th line of Table 5, degradation of the engine performance by the noise is prevented. About this, it is as above-mentioned. Moreover, according to the example shown in the 7th line of Table 5, and the 8th line, it is effective in a manufacturing cost being reduced by manufacturing the circuit on each semiconductor chip according to the optimal manufacture process for each.

[0070] (Example 1) Below, the 1st example of the semiconductor device by this invention is explained at a detail.

[0071] The example of a configuration of the semiconductor memory of this example is shown in drawing 9 . Drawing 9 shows the configuration of DRAM, and each circuitry element is the same as that of drawing 1 , and gives the same number to each. DRAM80 consists of semiconductor chips with which the memory core section 50 differs from the memory circumference circuit section 60. The memory core section chip 50 consists of the sense amplifier 4 arranged in the same pitch as the memory cell array 1 and the memory cell in this memory cell array 1, the column selector 3, a column decoder 2, a WORD driver 6, and a low decoder 5. As an I/O signal to this memory core section chip 50 The PURIDE code address input signal XAi to the low decoder 5 55, the PURIDE code address input signal YAi(23:0) 52 to the column decoder 2, the data I/O signal Dco(7:0) 51 to the column selector 3, the substrate potential input VBB56, the pressure-up potential input VPP55, cel plate potential (27:0) And the bit line precharge potential inputs VBP and VCP54 and the power-source inputs VCC57 and VSS58, and a pan have the control signal input of what book which is not illustrated.

[0072] The memory circumference circuit section chip 60 The row address buffer 10, the column address buffer 9, the row address counter 11, the low pulley decoder 8, the column PURIDE coder 7, the data input output buffers 12 and 13, a light amplifier 14, the lead amplifier 15, the RAS system CAS system clock generation circuit 16, WE system

clock generation circuit 17 and OE system clock generation circuit 18 -- and It consists of a pressure-up potential generating circuit 19, a substrate potential generating circuit 20, and 1 / 2VCC generating circuit 21. As an I/O signal to this memory circumference circuit section chip 60 As an external signal over DRAM80, the address input signal A (10:0) 32, the data I/O signal DQ(7:0) 36, the RAS input signal 30, the CAS input signal 31, the WE input signal 35, the OE input signal 37, and power sources VCC33 and VSS34, As a signal between the memory core section chips 50 The PURIDE code address output signal XAo of the low pulley decoder 8 63, the PURIDE code address output signal YAo(23:0) 62 of the column PURIDE coder 7, the data I/O signal Dpe(7:0) 61 to a data line, the substrate potential generating circuit output VBB66, the pressure-up potential generating circuit output VPP65, the 1 / 2VCC generating circuit output VCP, (27:0) There is a control signal output of what book which is not illustrated in VBP64 and a pan.

[0073] DRAM80 realizes the same function as DRAM95 shown in drawing 1 by connecting the required signal between the memory core section chip 50 and the memory circumference circuit section chip 60.

[0074] Drawing 10 shows the example of a chip layout of the memory core section chip 50 in DRAM80 divided into the memory core section chip 50 and the memory circumference circuit section chip 60 as shown in drawing 9 , and the example of mounting of both chips. The memory core section chip 50 is manufactured using the DRAM process, and the memory cell array 1, the sense amplifier 3, the column selector 4, the low decoder 6, and the WORD driver 5 are arranged. Although the memory plate with which the memory cell array 1 was quadrisected, the low decoder 6, and the WORD driver 5 are the same layouts as drawing 2 , one column decoder 2 is arranged in common to a memory plate on either side, and the column selector selection signal which is the output of the column decoder 2 is wired common to the column selector in a memory plate on either side.

[0075] The circuit shown in the memory circumference circuit section 60 in drawing 9 is arranged, and the memory circumference circuit section chip 60 is manufactured in a different process from the DRAM process used for manufacture of the memory core section chip 50 like a logic LSI process. The memory circumference circuit section chip 60 and the memory core section chip 50 are mounted in a common substrate 81, and DRAM80 in drawing 9 is constituted by connecting the connection during both chips with the wye YABODO wiring 82. Moreover, the pad 83 for connecting an external focus is arranged at the memory circumference circuit section chip 60, mounts the DRAM configuration shown in this drawing 10 in the same package as the conventional DRAM, and connects the pad and external pin in the pad formation section 83 arranged at the memory circumference circuit section chip 60.

[0076] Here, the connection signal number between the memory circumference circuit section chip 60 and the memory core section chip 50 can become about 60 in 16 M bit DRAM in a configuration of being shown in drawing 9 , and the connection using the wire bond wiring 82 as shown in drawing 10 can realize it by the low price. When making connection between chips with still more numbers, the method which mounts a chip in a substrate by the bump can realize easily using a wiring substrate.

[0077] Since it becomes possible to manufacture only the memory core section chip 50 using an expensive memory process, and to use a cheap logic LSI process for manufacture of the memory circumference circuit section chip 60 by considering as such a memory configuration, cheap DRAM is realizable.

[0078] Moreover, while the memory core section chip 50 makes a semi-conductor substrate the substrate potential VBB for the improvement in the engine performance of DRAM and it can make substrate potential of the memory circumference circuit section chip 60 touch-down potential like Logic LSI Since the circuit element by which direct continuation is carried out to the external pin of a package will exist only in the memory circumference circuit section chip 60 a latch rise -- DRAM using a detailed-ized process while being able to wear, being able to make surge resistance be the same as that of Logic LSI and being able to make area of a protection network small -- also setting -- a latch rise -- it can wear and the measures against a surge can be taken easy. In addition, although constituted by each of the memory core section chip 50 shown in drawing 10 , and the memory circumference circuit section chip 60 with each circuit element shown in drawing 9 By what kind of circuitry the memory core section chip 50 and the memory circumference circuit section chip 60 are manufactured Depending on the block division method of memory, the wiring number during a chip, etc., assignment for the memory core section chip 50 of the optimal circuitry element and the memory circumference circuit section chip 60 is dependent on the requirement specification of memory to realize.

[0079] Moreover, in old explanation, although a cheap DRAM implementation means by this invention to realize using a semi-conductor manufacture process which is different in the memory circumference circuit section chip 60 and the memory core section chip 50 has been described, also in semiconductor memory, such as SRAM other than DRAM, EEPROM, and a flash memory, it can guess easily that the same effectiveness can be attained by using the memory implementation means shown in drawing 9 and drawing 10 .

[0080] (Example 2) In drawing 9 and drawing 10 , although the memory implementation means in the case of using one memory core was shown, when the memory of the capacity which a system needs is unrealizable with one chip, in the system using memory, a system will be realized using the memory of two or more chips. The 2nd example of a configuration in the semiconductor memory of this invention which constitutes the memory core section and the

memory circumference circuit section in the case where two or more memory cores are used for drawing 11 from a different chip is shown, and the example in the case of using two memory core section chips is shown in drawing 11 . 121-1,121-2 is the memory core section chip equipped with the same element circuit as the memory core section chip shown in drawing 9 , respectively, and it equips each I/O signal of this memory core section chip 121-1,121-2 with buffers 67-69, and it is controlled so that chip select signal CS 59-1 and 59-2 are activated. 122 is a circumference circuit chip, and except that two chip select signals (CS1, CS2) 38 and 39 are crossing the chip, it is the same as that of the circumference circuit chip shown in drawing 9 . The memory core section chip 121-1,121-2 and the circumference circuit chip 122 are mounted in a substrate, and the example which connected between each chip is shown in drawing 12 . The memory core section chip 121-1,121-2 and the circumference circuit chip 122 are mounted in a substrate 120, and each signal pad is connected to the substrate 120 by the wire bond 82. Except for chip select signal CS, common connection of the memory core section chip 121-1 and the signal line of 121-2 is made with the wiring 131 on a substrate, and they are connected with the circumference circuit chip 122. The memory core section chip 121-1 and chip select signal CS of 121-2 are independently connected with the chip select signals (CS1, CS2) 38 and 39 of the circumference circuit chip 122, respectively.

[0081] In accessing the memory core section chip 121-1 from the exterior, while giving a signal required for RAS (30), CAS (31), WE (35), and OE (37), a selection signal is given to CS1 (38), the signal-line buffers 67-69 of the memory core section chip 121-1 are activated, and a required signal is given to a memory core and it accesses it. Since the selection signal is not given to CS2 (39) at this time, the signal-line buffers 67-69 of the memory core section chip 121-2 are not activated, and access to a memory core is not performed. Therefore, a chip select signal (CS1, CS2) is generated by 1 bit of the address to memory, and access to all the rooms that consist of a memory core section chip 121-1 and 121-2 can be performed by giving the remaining address to an address terminal 32.

[0082] In drawing 11 and drawing 12 , although the case where two memory core section chips are used has been explained, when using much memory core section chips further, and only the number of memory core section chips is equipped with the chip select signal given to a memory circumference circuit, it can be understood easily that the same function is realizable.

[0083] Thus, when using two or more memory core section chips by considering as drawing 11 and the configuration shown drawing 12 , it becomes possible to share a memory circumference circuit.

[0084] As stated above, cheap semiconductor memory is realizable by dividing and manufacturing semiconductor memory for a memory core section chip and a memory circumference circuit section chip, and connecting both chips with a mounting means.

[0085] (Example 3) Memory is used with other LSI, such as signal processing LSI, constitutes the system, and explains the optimal semiconductor device implementation means in a system level including such memory and signal processing LSI below.

[0086] In realizing a signal processing system, the signal-processing chip and semiconductor memory which were integrated serve as an indispensable existence. Therefore, the signal processing system is realized combining two or more signal-processing chip and two or more memory chips.

[0087] On the other hand, bare chip mounting by MCM prospers as a technique for the miniaturization of systems, such as a pocket device. MCM mounts an LSI chip in a substrate as [bare chip], and connects between LSI chips using various approaches.

[0088] The 1st example of a configuration of the semiconductor device in this invention in the system which used semiconductor memory and a signal-processing chip for drawing 13 is shown, and it is considering as the example using DRAM as semiconductor memory. In drawing 13 , 200 is the circuit board and the DRAM core section chip 201 and the signal-processing chip 202 are mounted. The DRAM core section chip 201 serves as circuitry shown in the memory core section 50 in drawing 9 , and is manufactured in a memory process. Since the signal-processing chip 202 is equipped with the pad formation section 204 for making connection with the digital disposal circuit 206 which performs logical operation etc., the DRAM circumference circuit section 203, and an external pin, the digital disposal circuit 206 in the signal-processing chip 202 performs logical operation and the DRAM circumference circuit section 203 serves as circuitry shown in the memory circumference circuit section 60 in drawing 9 , this signal-processing chip 202 is a chip which can be manufactured in a logic LSI process. The required connection between this DRAM circumference circuit section 203 and the DRAM core section chip 201 is connected with the wire bond wiring 208. Here, when the memory space which a system needs is 2 M bytes, the memory space of a DRAM core section chip can become 16M bit, and one chip can realize it in the present semi-conductor manufacturing technology. When performing bit width of face of the data transfer between a digital disposal circuit 206 and memory by 8 bits, like explanation by drawing 10 , the signal-line connection number between the DRAM circumference circuit section 203 and the DRAM core section chip 201 can become about 70, and can be realized by connection with wire bond as shown by a diagram.

[0089] In such a configuration, a digital disposal circuit 206 will give the address and a control signal to the DRAM circumference circuit section 203 in the same chip, and will output [when the digital disposal circuit 206 in the signal-processing chip 202 accesses DRAM] and input data.
[0090] By considering as such a configuration, the DRAM core section chip 201 realized using an expensive process serves as only the memory core section arranged in the pitch of a memory cell, and can realize the DRAM circumference circuit section 203 in a cheap semi-conductor manufacture process compared with a memory process together with a digital disposal circuit 206. When the digital disposal circuit 206 in the signal-processing chip 202 is large-scale, compared with the case where the DRAM circumference circuit section 203 is not included, the rate of the increment in a chip size of the signal-processing chip 202 is very small. Therefore, the fall of the manufacture yield by having included the DRAM circumference circuit 203 and the rise of chip cost are very small similarly, and a cheap system can be realized.
[0091] Since a signal-processing chip and a memory chip can be connected now with much wiring by using an MCM technique as mentioned above, a highly efficient signal processing system is realizable with a cheap configuration by using this MCM technique.
[0092] (Example 4) Drawing 14 shows the 2nd example of a configuration of the semiconductor device in this invention which constitutes the signal processing system which used semiconductor memory and a signal-processing chip using an MCM technique. In drawing, the example of the system using DRAM as semiconductor memory is shown. The signal-processing chip 302 is equipped with the core based CPU 303 which calculates, and is equipped with the data cache memory 304 and the instruction memory 305 for improvement in the speed of access with memory. When access to the data cache memory 304 and the instruction cache memory 305 from a core based CPU 303 is a mistake hit, in order to replace the block data in this data cache memory 304 and the instruction memory 305 with the data of the DRAM chip 301, it is necessary to transmit a lot of data between the DRAM chip 301, the data cache memory 304, and the instruction memory 305. Since this transfer time influences the processing engine performance of a system, to transmit for a short time is demanded.
[0093] Here, when the memory space which a system needs is 2 M bytes, the memory space of the DRAM chip 301 is 16M bit, and the technique realizable [with one chip] is established in the present semi-conductor manufacturing technology. In the conventional 16 M bit DRAM, data I/O bit width of face is about 8-16 bits as mentioned above in consideration of increase of the power consumption by load-carrying capacity drive, and a noise etc. Moreover, since the data pin terminal capacity of packed DRAM which is shown in drawing 3 is set to about 5pF as mentioned above and the data pin terminal capacity of signal processing LSI also serves as a comparable value, in mounting to the printed-circuit board of the signal processing LSI and DRAM shown in drawing 3 , it is set to about 15pF as the sum total of each terminal capacity and printed-circuit capacity as a capacity of the data line to which signal processing LSI and DRAM is connected. On the other hand, it sets in the configuration shown in drawing 14 . Since each chip can be manufactured on the assumption that mounting by MCM, the data pin of signal processing LSI and DRAM Since it is not necessary to enlarge transistor size of an input output buffer and since external load-carrying capacity is limited, and direct continuation is not carried out to an external pin, when a surge protection device becomes unnecessary, terminal capacity of a data pin can be set to about 1pF, respectively. Therefore, since the capacity of the data line to which signal processing LSI and DRAM is connected is set to about 2pF, when it considers as 60-120 bits as the number of data pins, the power consumption for a data pin capacity drive becomes the same as that of the case of mounting by drawing 3 .
[0094] Therefore, in order to perform high-speed data transfer between the signal-processing chip 302 and the DRAM chip 301 by considering as the configuration shown in drawing 14 For both chips, it has two or more data terminals, and it becomes possible to perform two or more data transfers to coincidence. When access to the data cache memory 304 and the instruction memory 305 from a core based CPU 303 is a mistake hit as mentioned above Since a data transfer rate can be enlarged between the DRAM chips 301, the system of high performance is realizable.
[0095] Thus, since it becomes possible to connect a signal-processing chip and a memory chip with much wiring in LSI implementation by the system configuration using an MCM technique as shown in drawing 14 , high-speed data transfer is realizable by preparing two or more data terminals in each of the signal-processing chip 302 and the DRAM chip 301, and transmitting two or more data to coincidence.
[0096] (Example 5) The 3rd example of a system configuration of the semiconductor device in this invention which realizes a low battery and low-power actuation for two or more data using such an MCM technique in the system in which a coincidence transfer is possible is explained below.
[0097] Drawing 15 shows the 3rd example of a configuration of the semiconductor device in this invention, and is an example of the structure of a system using semiconductor memory, two or more data transfer between signal processing LSI, and the parallel processing in signal processing LSI. In drawing, the example of the system using DRAM as semiconductor memory is shown. In order to perform data transfer in two or more data between the DRAM chips 401,

each of the DRAM chip 401 and the signal-processing chip 402 has offered two or more data terminals, and the signal-processing chip 402 has connected between the signal-processing chip 402 and the DRAM chips 401 with much wire bond wiring 406, while being equipped with two cores based CPU 403 and 404, in order to perform parallel processing.

[0098] In the signal processing system of such a configuration, a processing system is 8-bit architecture, and when performing processing whose cores based CPU 403 and 404 are 8 bits, respectively, two data can be processed to coincidence by cores based CPU 403 and 404 by performing data transfer between the DRAM chips 401 by 16 bits. Therefore, as compared with 8 bit-data transfer with the signal processing LSI and DRAM in a configuration of being shown in drawing 3 , and 8-bit signal processing in signal processing LSI, it can consider as a twice as many throughput as this.

[0099] Moreover, in the system configuration shown in drawing 15 , in realizing the same throughput as the system configuration in drawing 3 , it becomes possible to reduce power consumption sharply. The supply voltage dependency of the gate delay in the logic gate used with the signal-processing chip 402 and the supply voltage dependency of the access time in the DRAM chip 401 are shown in drawing 16 (a) and (b). A logic gate (a) and DRAM (b) of the electrical potential difference which serves as twice as many delay as this to delay by supply voltage 3.3V generally used conventionally are about 1.9V. Therefore, according to the system configuration shown in drawing 15 which performs data transfer with the DRAM chip 401 by 2 words, and performs juxtaposition signal processing by two cores based CPU 403 and 404, and which is depended signal-processing chip 402, the same processing engine performance as the system configuration shown in drawing 3 in 3.3V actuation using the supply voltage of 1.9V is realizable.

[0100] The comparison of the 3rd example of a system configuration in the semiconductor device of this invention shown by drawing 15 and the conventional system configuration is shown in drawing 17 . In drawing, the general-purpose chip MCM of what mounts the memory and signal processing LSI which were packed as shown in discrete ****3 of a system configuration 1 on a printed circuit board, and a system configuration 2 is the system mounted with the MCM technique using a conventional memory chip and a conventional signal-processing chip, and this invention of a system configuration 3 is the 3rd example of a system configuration in the semiconductor device of this invention shown in drawing 15 . A characteristic thing performs data transfer between a signal-processing chip and memory to two or more data coincidence, is performing parallel processing, and is operating [with the system configuration 3] by 10MHz by the system configuration 3 to operating by 20MHz with the system configuration 1 and the system configuration 2. However, since juxtaposition actuation is performed in the system configuration 3, the same system performance as a system configuration 1 and a system configuration 2 has been realized. Therefore, although the system configuration 1 and the system configuration 2 are operating by supply voltage 3.3V, a system configuration 3 can operate by 1.9V. Thereby, to power consumption being about 1W, a system configuration 1 and a system configuration 2 will operate by about 250mW, and the system configuration 3 has realized about 1/of identity ability with the power of 4.

[0101] Thus, the system of a low battery and a low power is realizable by using two or more data transfers and parallel processing using an MCM technique of this invention.

[0102] (Example 6) Drawing 18 shows the 4th example of a configuration of the semiconductor device in this invention which realizes the system using two or more data transfers and parallel processing which used the MCM technique by the low price. Drawing shows examples of the structure of a system, such as a Personal Digital Assistant using DRAM, flash memory, and signal-processing chip which were constituted using the MCM technique. The signal-processing chip 102, the DRAM core section chip 101, and the flash memory core section chip 103 are mounted in the common substrate 100, and the signal-processing chip 102 is equipped with the DRAM circumference circuit section 104 and the flash memory circumference circuit section 105 while it is equipped with two cores based CPU 107 and 108, in order to perform parallel processing. Furthermore, in order to perform data transfer in two or more data between the signal-processing chip 102, the DRAM core section chip 101, and the flash memory core section chip 103 Each of the DRAM circumference circuit section 104 in the DRAM core section chip 101, the flash memory core section chip 103, and the signal-processing chip 102 and the flash memory circumference circuit section 105 has offered two or more data terminals. Between the signal-processing chip 102, the DRAM core section chip 101, and the flash memory core section chips 103 is connected with much wire bond wiring 110 and 111.

[0103] As drawing 15 - drawing 17 explained by considering as such a configuration, while the system of a low battery and a low power is realizable by using two or more data transfers and parallel processing using an MCM technique The DRAM core section chip 101 and the flash memory core section chip 103 which are realized using an expensive semi-conductor manufacture process like explanation by drawing 13 It can consider only as the memory core section arranged in the pitch of a memory cell. Since the DRAM circumference circuit section 104 and the flash memory circumference circuit section 105 are realizable in semi-conductor manufacture processes, such as a cheap logic LSI process, compared with a memory process on the same chip as a digital disposal circuit 106 or cores based CPU 107

and 108 It becomes possible to realize the system of a low battery and a low power cheaply.
[0104] As drawing 11 and drawing 12 explained, when using two or more memory core section chips of the same configuration, it is possible to share a memory circumference circuit. Similarly, by making the same the word configuration of the DRAM core chip 101 and the flash memory core section chip 103 in the semiconductor device using the MCM technique shown in drawing 18 , as shown in drawing 19 (a), it becomes possible to share the memory circumference circuit of a DRAM core chip and a flash memory core section chip. In drawing 19 (a), as for a DRAM core chip and 503, 501 is [a flash memory core section chip and 502] signal-processing chips, and the signal-processing chip 502 is equipped with a digital disposal circuit 506, cores based CPU 507 and 508, and the memory circumference circuit 504.
[0105] The detail configuration of the memory circumference circuit 504 is shown in drawing 19 (b). Since the DRAM core chip 501 and the flash memory core section chip 503 serve as different control, the memory circumference circuit 504 is equipped with the DRAM control circuit 520 and the flash memory control circuit 523, the DRAM control circuit 520 is controlled based on a RAS signal and a CAS signal, and the flash memory control circuit 523 is controlled based on the chip enable signal (CE). The address system circuit 521 which consists of the column address buffer 9 in drawing 9 , low ADOBAFFA 10, the row address counter 11, the column PURIDE coder 7, and the low pulley decoder 8, and the data system circuit 522 which consists of the data input buffer 12, the data output buffer 13, a light amplifier 14, and the lead amplifier 15 are shared with the DRAM core chip 501 and the flash memory core section chip 503.
[0106] The DRAM core chip 501, the signal-processing chip 502, and the flash memory core section chip 503 are mounted on a substrate 500, bonding of the signal terminal for connecting between each chip is carried out to a substrate 500 with the wire bond 510, and between each chip is connected by the wiring 511-513 on a substrate 500. A DRAM core control signal is connected to the DRAM core chip 501 by wiring 511 among the signal terminals of the memory circumference circuit 504, a flash memory control signal is connected to the flash memory core section chip 503 by wiring 512, and an address system and a data system signal are connected to the DRAM core chip 501 and the flash memory core section chip 503 by wiring 513.
[0107] When the signal-processing chip 502 reads data from the DRAM core chip 501, RAS, CAS, and OE signal are generated by the digital disposal circuit 506, and it is given with the address in the memory circumference circuit 504. By generating the PURIDE code address by the address system circuit 521, and giving to the DRAM core chip 501, the memory circumference circuit 504 reads data from a DRAM core, and outputs them to a digital disposal circuit 506 through the data system circuit 522 while it generates a DRAM core control signal by the DRAM control circuit 520 based on RAS, CAS, and OE signal. At this time, since CE is not given, a flash memory control signal is not generated but the flash memory core section chip 503 of the flash memory control circuit 523 is still a standby condition. When the signal-processing chip 502 reads data from the flash memory core section chip 503, CE and OE signal are generated by the digital disposal circuit 506, and it is given with the address in the memory circumference circuit 504. By generating the PURIDE code address by the address system circuit 521, and giving to the flash memory core section chip 503, the memory circumference circuit 504 reads data from a flash memory core, and outputs them to a digital disposal circuit 506 through the data system circuit 522 while it generates a flash memory core control signal by the flash memory control circuit 523 based on CE and OE signal. At this time, since RAS and CAS are not given, a DRAM control signal is not generated but the DRAM core chip 501 of the DRAM control circuit 520 is still a standby condition. The data writing to the DRAM core chip 501 or the flash memory core section chip 503 from the signal-processing chip 502 can be similarly written in either the DRAM core chip 501 or the flash memory core section chip 503 by giving any of RAS and CAS, or CE signal they are to the memory circumference circuit 504.
[0108] In drawing 19 , although the word configuration of the memory core section of the DRAM core chip 501 and the flash memory core section chip 503 was explained about the case where identitas is carried out, when word configurations differ, it can be understood easily that it is possible to share a part of a part of the column address buffer in the address system circuit 521, row address buffer, column PURIDE coder and low pulley decoder, and the data input buffer in the data system circuit 522, data output buffer, lead amplifier, and light amplifier.
[0109] Thus, when using two or more memory of a different class, it becomes possible by realizing the memory core section and the memory circumference circuit section with a different chip to share a part of memory circumference circuit.
[0110] In the above-mentioned example, although this invention has been explained about DRAM, as stated first, this invention is not limited to DRAM. It is because having explained the example to the detail had strongly the common sense that the memory core section of DRAM and the memory circumference circuit section should be formed on the same semiconductor chip, about DRAM, so it is most suitable for explanation of the example of forming in a different semiconductor chip from this memory core section and the memory circumference circuit section expressing the description of invention. Moreover, this invention is not limited to MCM.

[0111] Below, how to divide a circuit block into two or more semiconductor chips is explained, referring to a drawing.
[0112] Drawing 20 (a) and (b) are the block diagrams showing the configuration of general MCU902 for control, and MCU903 for image processings.
[0113] First, the block parameter which shows the circuit information on MCU902 for control and the description of each configuration block is extracted, and it reads into CAD. Next, hierarchy expansion of a block is performed until grouping becomes possible. For example, LSI0 is developed to a MCU core, serial I/F, ROM and RAM, a timer, interrupt control, D/A, and each circuit block of A/D.
[0114] Next, grouping of the circuit block by which hierarchy expansion was carried out is carried out by making a difference of a "MCU core" and a "circumference circuit" into a parameter.
[0115] In the case of this example, as a group of LSI1, the circuit block of a MCU core will be chosen, and serial I/F, ROM and RAM, a timer, interrupt control, D/A, and the circuit block of A/D will be chosen as a group of LSI2, consequently hierarchies LSI1 and LSI2 will be generated.
[0116] Hierarchies LSI1 and LSI2 are generable also about MCU for image processings with the same procedure.
[0117] Drawing 21 (a) shows typically the condition of having separated the MCU core 905 and the circumference circuit 904, from MCU902 for control, and MCU903 for image processings, and drawing 21 (b) shows typically the cross section of the semiconductor device to which the chip 905 for MCU cores and the chip 904 for circumference circuits were connected with the MCM technique.
[0118] Drawing 22 (a) shows the case where the circuit block of a MCU core, and ROM and RAM was chosen, and serial I/F, a timer, interrupt control, D/A, and the circuit block of A/D are chosen as a group of LSI2 as a group of LSI1 on the occasion of grouping. Drawing 21 (b) shows typically the cross section of the semiconductor device to which the MCU core, the chip 908 for the common section, and the chip 907 (909) for circumference circuits were connected with the MCM technique.
[0119] In this way, there are the following advantages by dividing a circuit into a "MCU core chip" or "the chip for a MCU core and the common section", and a circumference circuit chip.
[0120] That is, if the circuit block common to two kinds of MCU(s) is formed on one semiconductor chip, the circuit area of the semiconductor device formed from two chips will contract as a whole, and the manufacture yield will also improve. Moreover, when designing MCU newly or performing a design change, if only a circumference circuit small-scale in comparison is newly designed or the design change of the design of a MCU core is carried out, it is sufficient for it, without changing. Since what is necessary is to perform only the test of the circumference circuit designed newly, it becomes unnecessary moreover, to newly prepare the circuit for a test. For this reason, the development cost as the whole semiconductor device is reduced.
[0121]
[Effect of the Invention] The various problems which produce the circuit which consists of circuit blocks with a different block parameter from being accumulated on one semiconductor chip are solvable by according to this invention, forming the 1st circuit block and the 2nd circuit block with which block parameters differ on a respectively different semiconductor chip, and connecting them electrically.
[0122] Since it becomes possible to manufacture only a memory core section chip using an expensive memory process, and to use a cheap logic LSI process for manufacture of a memory circumference circuit section chip by separating into the memory core section chip especially realized using the 1st semi-conductor manufacture process, and the memory circumference circuit section chip realized using the 2nd different semi-conductor manufacture process from the 1st semi-conductor manufacture process, it is effective in low-pricing of semiconductor memory.
[0123] Furthermore, the memory core section chip realized using an expensive process can be made only into the memory core section arranged in the pitch of a memory cell, and the memory circumference circuit section can be realized in a cheap semi-conductor manufacture process compared with a memory process to digital-disposal-circuit 1 clue. For this reason, when the digital disposal circuit in a signal-processing chip is large-scale, since it is very small, the fall of the manufacture yield by the rate of the increment in a chip size having become very small, and having included the memory circumference circuit section compared with the case where the memory circumference circuit section is not included, as for the signal-processing chip, and the rise of chip cost are effective in low-pricing of the semiconductor device which constitutes a system similarly.
[0124] The memory core section chip containing the memory cell for memorizing the data realized using the 1st semi-conductor manufacture process, By connecting the signal-processing chip which carries the digital disposal circuit which processes using the data memorized by the memory circumference circuit section and the memory core section chip which are realized using the 2nd different semi-conductor manufacture process from the 1st semi-conductor manufacture process High-speed data transfer becomes possible between a signal-processing chip and a memory chip, and it is effective in high-performance-izing of a system. Furthermore, while it is very effective in the low battery and low-power-izing of a system by using two or more data transfers and parallel processing, also in a low price, it becomes

effective.

[Translation done.]